Functional and structural integration for advanced modular motor drives

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Abstract

Traditionally, motor drive systems require separate space due to the volume of the cooling system and power electronics. As a result, long cables were used to connect the motor and the inverter. However, these long cables caused issues such as Electromagnetic interference problems, poor reliability, additional electricity loss, and increased cost. In modern applications, where motors are used in various fields, significant efforts have been made to reduce the volume of the drive system in many studies. The ultimate goal of these studies is the physical integration of the motor and the inverter. If physical integration is achieved, the volume of the motor drive can be greatly reduced by increasing the power density. Furthermore, the motor drive doesn't need long cables between the motor and the inverter, which is very helpful in resolving the problems mentioned above.

To realize these forward-looking ideas, new research is needed on wide-band-gap power semiconductors that enable high-temperature operation and high-speed switching, as well as on special power module packaging technologies and topologies that can increase power density using these semiconductors. Additionally, research on motor control using high-speed switching is required.

Therefore, this study reviewed high-power density topologies using wide-band-gap semiconductors and designed an original bidirectional power module that can be physically integrated with the motor wire and operate at temperatures up to 200 degrees Celsius. Based on this, a novel current controller without a motor current measured sensor, suitable for a wide-band-gap-based current source inverter, was proposed and implemented to increase the power density further.

Keywords: Power electronics, Motor drives, Current Source Inverter (CSI), Silicon Carbide (SiC), Integrated Motor Drive (IMD), Power Module, Power Overlay, Motor control algorithm

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ASD	:	Adjustable Speed motor Drive
Ag	:	Silver
Al	:	Aluminum
EMI	:	Electro Magnetic Interference
IMD	:	Integrated Motor Drive
IMMD	:	Integrated Modular Motor Drive
IMS	:	Insulated Metal Substrate
POL	:	Power Overlay
CSI	:	Current Source Inverter or Current Source Inversion
VSI	:	Voltage Source Inverter
PWM	:	Pulse Width Modulation
WBG	:	Wide-Band-Gap
GaN	:	Gallium nitride
Si	:	Silicon
SiC	:	Silicon carbide
FPGA	:	Field Programmable Gate Array
CTE	:	Coefficient of Thermal Expansion
HEMT	:	High-Electron Mobility Transistor
SVM	:	Space Vector Modulation

RB	:	Reverse blocking
BD	:	Bi-directional
BDS	:	Bi-directional Switch
POL	:	Power Overlay
IMS	:	Insulated Metal Substrate
FOC	:	Field Oriented Control
PMSM	:	Permanent Magnet Synchronous Motor

1. INTRODUCTION

In the past three decades, there has been significant advancement in motor drive systems. Typically, electric motors are used to convert electrical energy into mechanical energy, and due to industrial advancements, electric motor drive systems now account for over 40% of global energy consumption [1]. The emergence of various applications, such as household appliances and electric vehicles, utilizing precise position control and variable speed adjustments, has contributed to the expanding scale of the industry. Moreover, these systems are widely employed across a broad power range, from a few watts to megawatts. Therefore, even minor improvements in motor drive systems can lead to substantial economic and environmental changes in modern societies [2-4].

For this reason, in many applications over the past decade, electric motor drive systems have replaced fixed-speed motors with adjustable-speed drives that can control torque and speed according to mechanical loads and environmental factors. Consequently, due to higher efficiency and power density, the traditional induction motors have been replaced by permanent magnet synchronous motors suitable for variable speed in many industrial sectors.

However, replacing fixed-speed motors with adjustable-speed motor drives requires additional significant costs and space for the drive. The motor drive systems consist of separate inverters and motors connected via long cables. Inverters are comprised of passive components (inductors and capacitors), power semiconductors, interconnection lines, sensors for voltage, current, temperature, and control devices, as well as heat dissipation devices and space for cooling. Hence, inverters require substantial space.

Advancements in various technological fields indicate new directions for these traditional motor drive systems. There is a growing demand for mobility using batteries, small household appliances, and air conditioners requiring high temperature and efficiency. This demand for miniaturization and increased power density drives the market toward the future concept of Integrated Motor Drive (IMD) [5-7].

Integrated Motor Drive (IMD) systems, which integrate the motor, control, and drive circuits into a single enclosure, offer a new paradigm in high-power-density motor drive structures. This integration brings forth a host of advantages. Inefficient fixed-speed motors can be replaced without mechanical alterations, potentially reducing costs by eliminating long connecting wires that can cause Electro Magnetic Interference (EMI) issues. However, the most significant benefit is the reduction in system mass and volume. For instance, shrinking the drive's volume in electric cars can boost battery capacity or interior space. Similarly, handheld vacuum cleaners can shed weight by using IMDs. For air conditioners, downsizing control boxes can increase the heat exchanger area or secure more maintenance space. Thus, compacting motor drive systems can significantly enhance system performance, as these examples illustrate.

However, the structural integration of power converters and motors poses technical challenges in design and manufacturing based on mechanical and thermal analyses. Placing power converters near motors leads to thermal management issues, and despite the appealing advantages, practical applications have been limited due to the volume of power electronics. The recent surge in Wide-Band Gap (WBG) power semiconductors, primarily propelled by the electric vehicle industry, holds immense potential. These semiconductors, with their ability to offer lower switching losses and higher operating temperatures, can pave the way for functionally and structurally new designs that can transcend the constraints of traditional silicon-based power converters. By significantly boosting the switching frequency of power semiconductors, it becomes feasible to reduce the size of passive components of power converters and explore innovative cooling designs, capitalizing on their high-temperature operation characteristics.

Therefore, this study is about functionally new topologies suitable for integrated motor drive (IMD) designs using next-generation WBG power semiconductors. Additionally, structural design methods to realize IMDs will be discussed. Finally, it also proposes new control methods based on high-speed switching.

1.1 Structural and Functional integration of motor-driven system

The most common Integrated Motor Drive structure is designed with power electronics mounted on the motor housing surface. This setup not only offers a significantly higher power density but also holds the potential to replace fixed-speed motors with Integrated Motor Drives that can fit into the same space. However, despite their compactness, the surface-mounted integration configurations remain physically independent from the motors to inverters. An advanced level of structural integration can be achieved by having a structure in which the stator of the motor and the power electronic module are physically coupled [5-7].

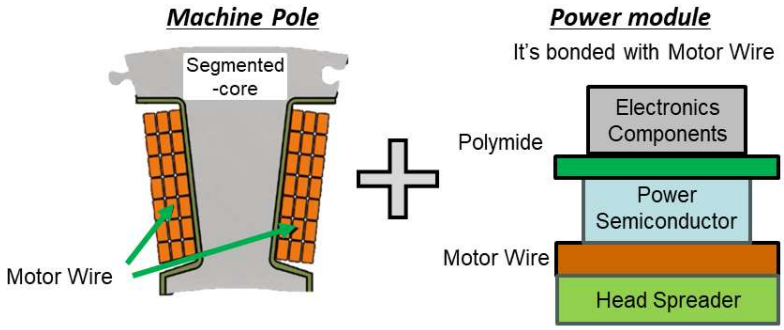


Figure 1. 1. Idea of single slot module concept of Integrated Modular Motor Drive (IMMD)

The Integrated Modular Motor Drive (IMMD) is a concept that addresses technical issues associated with the modularization of the stator and inverter. As you can see from Figure 1.1, the IMMD divides both the power electronics and the machine stator into individual phase segments. An individual stator segment with concentrated winding is physically integrated with a single-phase inverter module and its dedicated controller to form an integrated pole-drive unit [5-7]. These identical pole-drive units equal the number of concentrated stator windings in the machines. They are interconnected to form a ring-shaped stator assembly comprising the machine stator and the motor drive inverter.

This modularization offers several practical advantages [5-7]. First, it provides higher fault tolerance, ensuring the system continues to operate even when an individual module

fails. Second, it improves manufacturability, as each stator module is identical, making it an attractive candidate for high-volume manufacturing. Third, adopting segmented stator poles with concentrated windings offers the benefits of simplified stator pole windings, high slot fill factors, and short end-winding lengths. Finally, these modules are physically independent, allowing for easy connection in series or parallel for control, as shown in Figure 1.2 [8]. That is, it is possible to customize the power electronic circuit to achieve high-efficiency operation according to the motor load and speed. As a result, it is possible to implement an electrical gear similar to a mechanical gear in a vehicle.

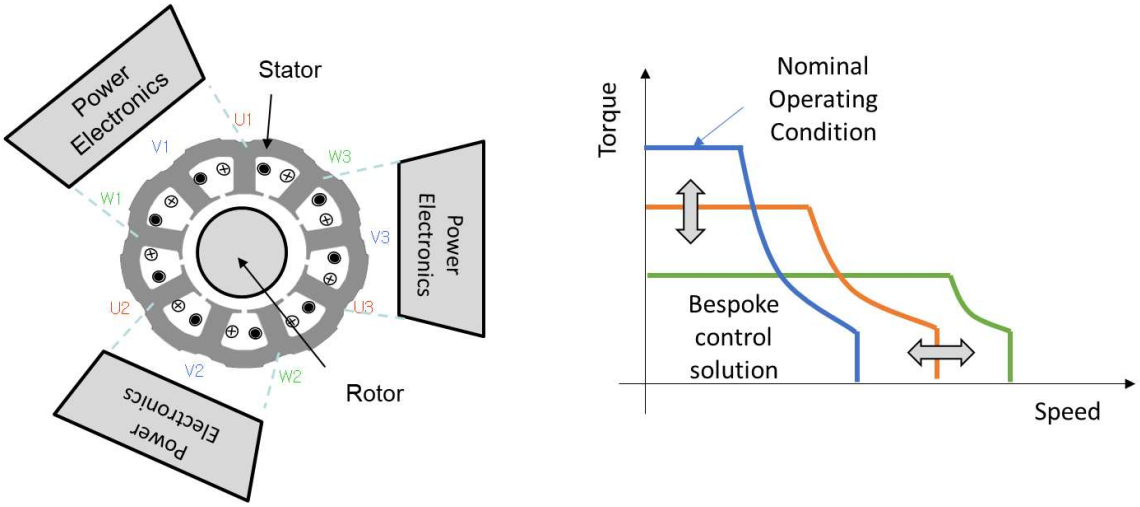


Figure 1. 2. Example of modular control for Integrated Modular Motor Drive-fed AC Machine

Most of these IMD methods have involved coupling a motor wire to a power electronic PCB module. In this study, we propose a novel integration method based on direct coupling to the power switch with motor wires, as shown on the right side of Figure 1.1. For specific applications, the integration of this unique structure can be considered based on the temperature of the motor wire and its cooling system, as shown in Figure 1.3.

For this unique structural integration, high-temperature operation is essential. Especially for direct connection with the motor, the maximum temperature of the motor wire must be considered. Generally, in many motor applications, the maximum temperature of the motor is managed within 135 degrees Celsius [9]. Depending on the type of magnets used in the motor, the maximum operating temperature varies, but for permanent solid magnets such

as NdFeB, it is around 60 to 150 degrees Celsius. However, maintaining magnetism at high temperatures increases costs, and the design temperature must be determined depending on the application to prevent demagnetization [10] .

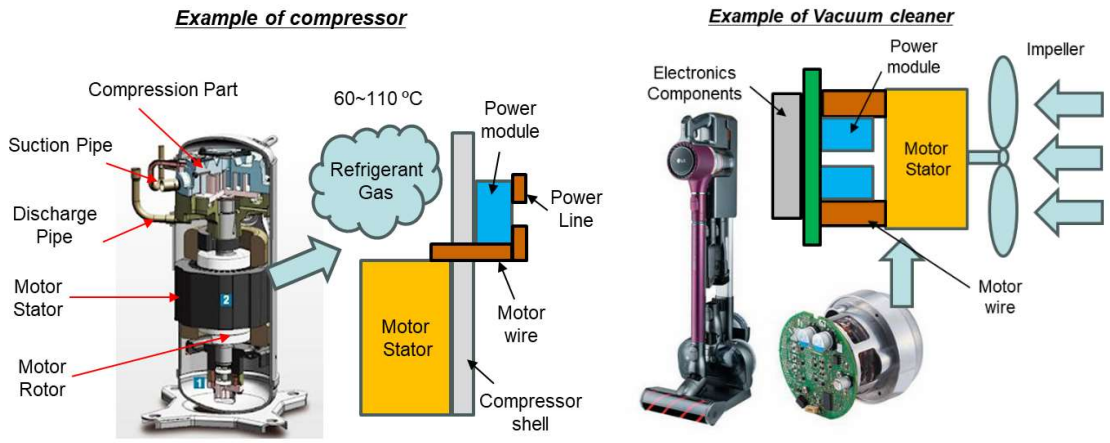


Figure 1. 3. Examples of direct motor-wire coupling IMDs

For example, refrigerant gases are managed in compressors at temperatures below 110~120 degrees Celsius [11]. Since high-temperature, high-pressure refrigerant gas cools the motor, the temperature of the motor wire can be assumed to be the same as that of the compressed refrigerant gas. Another example could be handheld vacuum cleaners [12]. In handheld vacuum cleaners, a propeller capable of generating strong airflow is connected to the motor, allowing for powerful forced cooling. The strong airflow also cools the motor. Therefore, the temperature of the motor is managed through this process. In both cases, the system provides strong heat dissipation performance, and the motor temperature can be managed within 135 degrees Celsius. In such cases, it can be noted that the boundary condition of the power switch for structural integration design should be considered within 135 degrees Celsius [13].

As a result, it is important to note that this technology has some challenges. These include the difficulty of mechanically and structurally integrating the modules with the motor from the high temperature and small volume of power electronics and the necessity for a complex control system for the individual power modules.

1.2 Research Motivation and Objectives

To overcome these technical challenges discussed in the above section, new approaches to power converters and packaging technologies using WBG power semiconductors are required.

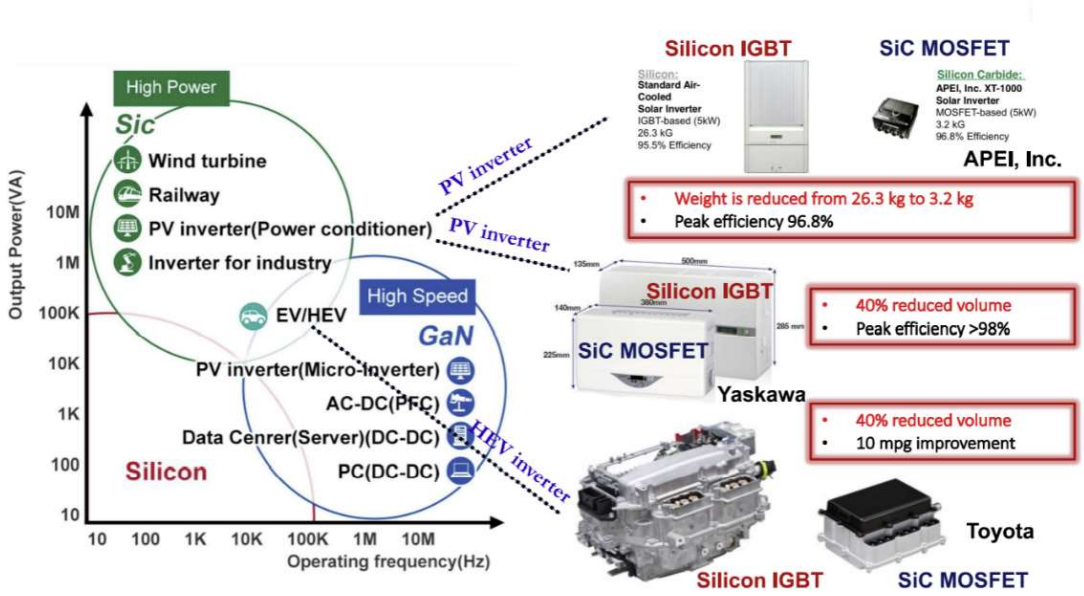


Figure 1. 4. Benefits of Wide Bandgap (WBG) Power Switching Devices [14-17]

Figure 1.3 shows some representative examples of the significant reduction in volume and mass using WBG power switches. The volume is reduced by about 40% while maintaining high efficiency due to the very low switching loss of the WBG power semiconductor.

One of the key advantages of WBG semiconductors is their superior switching speed, which outperforms Si-based semiconductors. This translates to minimal switching losses, enhancing efficiency and allowing for the reduction of the size of passive components. Alternatively, reduced switching losses can also be used to reduce the volume of the cooling system. This means smaller fans, heatsinks, and baseplates can be designed, which contributes to the overall reduction in mechanical weight and size of the system [18].

In the case of motor drives, this high-speed switching can increase the fundamental frequency of the motor, leading to an increase in the pole number. This, in turn, opens up new design opportunities for increasing motor power density. Moreover, increasing the bandwidth of controllers, reducing motor current ripple, decreasing motor losses associated with PWM, and mitigating torque ripple are among the potential improvements that the system can gain.

So far, silicon-based power semiconductors have dominated the market and are limited to maximum junction temperatures of up to 200 degrees Celsius. With their higher bandgaps than Si, Gallium Nitride (GaN) and Silicon Carbide (SiC) hold the promise of devices that can operate at temperatures as high as 600 degrees Celsius, a significant advancement [19-20].

However, replacing Si semiconductors with WBG semiconductors in the motor drive systems, mainly voltage source inverters, and increasing the switching frequency pose additional technical challenges. Firstly, the size of the DC link capacitor, which is one of the most sensitive components with considerable volume and reliability, is challenging to reduce significantly with the increase in switching frequency. Additionally, if the connection cable between the voltage source inverter and the motor is long in typical motor applications, increasing the switching frequency leads to higher voltage changes per unit time, resulting in increased power losses from long cables due to parasitic currents or causing EMI issues. This higher dv/dt (differential voltage at different times) can also increase motor insulation stress and negatively impact bearing life consumption.

Therefore, the first objective of this study is to explore topologies based on the WBG semiconductor with high-speed switching and a small volume of power electronics. To increase the power density of the motor-driven system by reducing the volume of the power converter using WBG and increasing the switching frequency, new topologies with more suitable features than the traditional voltage source inverter must be reconsidered.

Furthermore, to effectively implement IMMDs, where high-temperature operation is essential, designing physical power module packaging using WBG power semiconductors is necessary. While WBG semiconductors allow for high-temperature operation, traditional

structural packaging of power modules still faces challenges in increasing their operation temperature. This is where our research steps in, aiming to design a lightweight power switch capable of high-temperature operation suitable for integrated motor drives. Given the requirement for high-speed switching, our study also includes electromagnetic analysis along with electrothermal analysis.

The last objective of this study is to explore ways to reduce the complexity of control in functionally modular design by utilizing WBG's high-frequency switching. It seeks to minimize the number of sensors and proposes simplified control design strategies by using high-frequency switching and high-frequency sampling.

1.3 Outline of Thesis

Chapter 2 aims to present and analyze the wide bandgap (WBG) semiconductor and their applications for power electronics. This chapter will explore why this study focuses on power converters using WBG power semiconductors by examining their physical properties. Additionally, it will identify the issues associated with the traditionally used voltage source inverters when utilizing WBG semiconductors. Furthermore, it will review newly emerging power electronics topologies and discuss their suitability for integrated motor drive systems.

In **Chapter 3, t**he fundamental operating principles of the Current Source Inverter (CSI) are examined. This chapter covers switching patterns and Space Vector Modulation (SVM), providing detailed analysis and constructing a simulation model to illustrate these concepts.

In **Chapter** 4**,** we discuss design methods for physically integrated motor drivers, focusing on power switches using power semiconductors and their necessary physical properties. We review thermal modeling and propose two design approaches for the bidirectional power switches needed for WBG-based current source inverters. While bond wires are still required for chip connections, we considered lighter and more cost-effective Insulated Metal Substrate (IMS)-based switches compared to the traditional Double

Bonded Copper (DBC) method. However, we designed a new bidirectional power switch based on Power Overlay (POL) technology due to IMS's insulation layer and high-temperature limitations. This design eliminates the insulation layer, allowing the MOSFET's drain to be directly integrated with motor wires. Capable of operating at temperatures up to 200°C, this new power switch is suitable for integrated modular motor drive systems due to its small volume. We have also developed a prototype to demonstrate its potential.

Chapter 5 covers a simplified and robust control design based on high-frequency sampling. Leveraging high switching frequency enhances power density, opening up a new avenue of high-frequency sample-based control in motor drive systems. In modular designs, where multiple power electronic devices are typically connected in parallel, the number of sensors significantly impacts the system's complexity. In particular, current source inverters traditionally require voltage and current sensors, necessitating a complex controller structure. This study proposes a method to simplify the controller and reduce the number of current sensors by utilizing WBG semiconductors.

In **Chapter 6,** an experimental circuit is constructed using the discrete bidirectional power module designed in the previous chapter to implement the Buck-CSI. Based on the implemented Buck-CSI, the PMSM motor controller and the special PWM operation of the CSI are realized on an FPGA platform. The proposed AC current sensor-less control is then verified in the implemented Buck-CSI.

Finally, **Chapter 7** summarizes this thesis's main research achievements and conclusions. It also identifies and discusses future research areas.

2. Wide-Band-Gap Power Conversion for Motor-Drive Application

This chapter reviews the literature on WBG power semiconductors, which are essential for high-temperature operation and high-power density implementation. Since the 1950s, Wide Bandgap (WBG) semiconductors have been hailed as the future of semiconductor technology due to their ability to operate at high temperatures and their low conduction and switching losses. These properties make them ideal for applications requiring increased power density. Gallium Nitride (GaN) and Silicon Carbide (SiC) are emerging as significant technological and commercial competitors to traditional Silicon (Si) in the semiconductor market. Therefore, the physical properties of power semiconductors are analyzed, and the characteristics and advantages of WBG semiconductors are identified by comparing them with traditional Si. The suitability of WBG semiconductors for application in IMDs is then evaluated.

Furthermore, the application of WBG power semiconductors in motor drives requires identifying the issues with existing topologies and reviewing the newly emerging WBG-based topologies. This review will help select candidates that are more suitable for structural integration.

2.1 Review of Wide-Band-Gap Devices

The electrical performance of a semiconductor device is fundamentally linked to the material's physical properties. Electrons in solid materials occupy different energy bands around an atom. In a semiconductor, the conduction band is the energy band where free electrons can exist, and the valence band is the energy band immediately below it, where electrons are typically bound to atoms. Current conduction in a material occurs when electrons move through the conduction band from one atom to another. The movement of electrons leaves behind holes in the valence band, which also have a positive charge and can move through the material in the opposite direction of the electrons, contributing to current conduction. In semiconductors and insulators, the valence and conduction bands are separated by an energy band gap (Eg). In contrast, metals have a very small energy band gap, or the two bands overlap, effectively eliminating the band gap. The band gap represents the energy required for an electron to transition from the valence band to the conduction band, or vice versa. SiC and GaN have energy gaps more significant than 3 eV, classifying them as "wide bandgap" materials. This higher bandgap energy provides the basis for multiple advantages of WBG power devices, including lower on-resistance (R_{ON}), and much higher safe junction operating temperatures [21-23].

2.1.1 On-state performance

The total on-state current in a semiconductor device is the sum of the electron and hole current, which can include both drift and diffusion components [24-26]. The expression for this total current density can be written as

$$\vec{J} = q\mu_n n \cdot \vec{\nabla}V + qD_n \cdot \vec{\nabla}V + q\mu_p p \cdot \vec{\nabla}V - qD_p \cdot \vec{\nabla}p \tag{2.1}$$

Here, q represents the charge of an electron, μ_n and μ_p denote the mobilities of electrons and holes respectively, n and p are the electron and hole concentrations respectively, D_n and D_p stand for the diffusion coefficient for electrons and holes. The

term $\vec{\nabla}V$ is the electric field. In Eq. (2.1), $q\mu_n n \cdot \vec{\nabla}V$ and $q\mu_p p \cdot \vec{\nabla}V$ represent the drift current due to electrons and holes, respectively. Additionally, $qD_n \cdot \vec{\nabla}V$ and $-qD_p \cdot \vec{\nabla}p$ represent the diffusion current due to electrons and holes, respectively.

Based on Eq. (2.1) we can understand that the requirements for achieving high on-state performance in semiconductor devices include using materials with high doping levels, maximizing the components contributing to diffusion current, and reducing the physical thickness of the semiconductor structure.

High doping levels increase the concentration of charge carriers (electrons and holes). According to Eq. (2.1), the drift current components are directly proportional to the carrier concentrations. Higher doping levels enhance these drift current components, thus improving the overall current conduction.

The diffusion current components depend on the gradients of the carrier concentrations and the diffusion coefficients. By optimizing the material properties and device structure to create favorable concentration gradients, the diffusion current can be maximized. This is particularly important for devices operating under conditions where diffusion dominates over drift.

The physical thickness of the semiconductor affects the overall resistance and performance of the device. A thinner structure can reduce the distance over which carriers need to move, thus reducing resistance and improving current flow. This is reflected in the expression for specific on-resistance

$$r_{on} = \frac{1}{q\mu_n n} \cdot d \tag{2.2}$$

,where reducing thickness (d) decreases r_{on}, enhancing the on-state performance.

2.1.2 Off-state performance

The off-state performance in semiconductor devices is equally crucial as it determines the ability of the device to block current flow when it is supposed to be in a non-conductive state. Achieving high off-state performance involves different considerations compared to on-state performance [27-28].

The breakdown voltage (V_{BD}) is the maximum voltage that a device can withstand before it starts to conduct significantly in the off-state.

$$V_{BD} \propto \frac{1}{2} \cdot \frac{\varepsilon_r}{qn} \cdot E_{crit}^2 \tag{2.3}$$

This indicates that materials with high relative permittivity (ε_r) and critical breakdown electric field (E_{crit}) can achieve higher breakdown voltages. Additionally, lower doping concentrations (n) also contribute to higher breakdown voltage.

The depletion width (W_d) is another important factor in off-state performance. It can be expressed as

$$W_d \propto \sqrt{\frac{2\varepsilon_r}{qn} V_{BD}} \tag{2.4}$$

Thicker devices tend to have wider depletion regions, assuming the same doping concentration and material properties.

Therefore, in designing semiconductor devices, there is a trade-off between achieving a wide depletion width for high off-state performance and maintaining low on-resistance for efficient on-state performance. The key is to find an optimal doping concentration and device thickness that balance these requirements.

2.1.3 Switching performance

The switching performance of semiconductor devices is critical for applications requiring high efficiency and fast response times.

Thinner semiconductor devices reduce the distance that charge carriers need to travel, resulting in faster switching times. Additionally, thinner devices help minimize parasitic capacitance, which is essential for high-speed operation.

Low diffusion currents are essential to reduce unwanted charge carrier movement that can slow down the switching process. This can be achieved through material optimization and the use of lifetime controlling techniques, which manage the recombination rate of charge carriers, thus reducing diffusion currents.

The switching speed of a device is also influenced by the high-field saturation velocity of the charge carriers, which is a material characteristic. Materials with higher saturation velocities allow charge carriers to move faster under high electric fields, improving the switching speed of the device. The velocity of charge carriers directly affects the switching performance. Higher velocities result in quicker response times and more efficient switching. This velocity is determined by the material properties, such as electron and hole mobility.

$$\vec{v} = \frac{\mu\vec{E}}{1 + \frac{\mu\vec{E}}{\overrightarrow{v_{n.sat}}}} \tag{2.5}$$

This equation shows that the velocity of charge carriers ($\vec{v}$) increases with the electric field until it approaches the saturation velocity. Materials with higher saturation velocities ($\overrightarrow{v_{n.sat}}$) allow for higher charge carrier velocities, leading to improved switching performance.

The switching performance of semiconductor devices can be significantly enhanced by using thinner devices, reducing diffusion currents through lifetime controlling techniques,

and utilizing materials with high-field saturation velocities and high charge carriers' velocity.

2.1.4 Comparison WBG vs. Si

Table 2.1 compares the critical properties of the new semiconductor materials, Gallium Nitride (GaN) and Silicon Carbide (SiC), with conventional Silicon (Si) [29-34] .

Table 2. 1. Main physical properties of semiconductor materials [35-39]

Property	Symbol(unit)	Si	4H-SiC	GaN
Band gap	$E_g\ (eV)$	1.1	3.26	3.45
Electron mobility	μ_n (cm^2/Vs)	1400	800	2000
Hole mobility	μ_p (cm^2/Vs)	450	140	30
Intrinsic carrier concentration at 300K	n_i (cm^{-3})	$1.5x10^{10}$	$5x10^{-9}$	$1.9x10^{-10}$
Electron saturated velocity	v_{nsat} $(\times 10^7 cm/s)$	1.0	2.0	2.5
Critical breakdown electric field	E_{crit} (MV/cm)	0.25	2.2	3.5
Thermal conductivity	λ (W/cmK)	1.5	3.8	2.3

The WBG semiconductors, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), possess significantly higher critical breakdown electric field (E_{crit}) than Silicon. This attribute allows these materials to operate at much higher voltages based on Eq. (2.3). For a given voltage rating, much higher doping levels can be used in WBG semiconductors. This results in better on-state performance with reduced device thickness. The reduced thickness leads to decreased charge accumulation effects, which in turn enhances switching

performance. Additionally, higher saturation velocities ($V_{n.sat}$) of charge carriers in WBG materials favor faster switching and higher power devices from Eq. (2.5).

Conversely, for a given chip thickness, devices with much higher voltage ratings can be achieved with WBG semiconductors. This combination of higher doping levels and reduced thickness, enabled by the superior breakdown electric field strength of WBG materials, significantly improves the efficiency and effectiveness of semiconductor devices. Consequently, WBG semiconductors allow the production of higher power-rated devices that can be smaller in size, offering improved voltage-blocking capability.

Higher bandgap energy (E_g) and extremely low intrinsic carrier concentration (n_i) values enable stable temperature performance and high-temperature capability in WBG semiconductors. This means that devices can operate reliably at higher temperatures, although the limitation is their packaging technology. The higher bandgap energy also improves voltage-blocking performance at given temperatures and enhances avalanche ruggedness. This relationship can be expressed as

$$n_i^2(T_j) = C \cdot T_j^3 \cdot e^{-\frac{E_g(T_j)}{k \cdot T_j}} \tag{2.6}$$

where lower intrinsic carrier concentration results in lower leakage currents and better high-temperature stability. The leakage current (J_{LEAK}) is influenced by various factors and can be described as

$$J_{LEAK} \propto \sqrt{2q\varepsilon_r \cdot \frac{V_{REV}}{n}} \cdot \frac{n_i}{\tau_{SC}} + \frac{qD}{L} \cdot \frac{n_i^2}{n} \tag{2.7}$$

Where q is the charge of an electron, ε_r denotes the relative permittivity of the material, V_{REV} is the reverse voltage, n indicates the doping concentration, τ_{SC} is the carrier lifetime, D signifies the diffusion coefficient, L is the diffusion length. Based on those equations, WBG semiconductors, with their higher bandgap energies, exhibit significantly lower intrinsic carrier concentrations, leading to lower leakage currents and enhanced high-temperature performance.

Higher thermal conductivity allows for better heat dissipation, which is essential for maintaining device performance and reliability. Better heat dissipation leads to a lower thermal resistance for a given power dissipation. As a result, the variation of the junction temperature (ΔT) can be reduced as follows.

$$\Delta T = P_{diss} \cdot R_{th}, \qquad R_{th} \propto \frac{1}{\lambda} \tag{2.8}$$

Reducing the junction temperature variation (ΔT) improves the reliability and longevity of the devices. This property enables WBG devices to handle higher power densities and operate more reliably at elevated temperatures, making them ideal for advanced power electronics applications.

This WBG semiconductor makes them ideal for IMDs that require operation above 135°C. SiC and GaN can produce devices with practical temperature limits of up to 600°C, a significant advantage over Si's limit of 225°C. High PWM frequency makes it possible to reduce the size of inductors and capacitors, shrinking the total volume and mass of the motor drive system except for common-mode filtering. This is particularly important in the converter unit of IMDs, where high heat flux is generated over a small area. By using SiC-based Power Electronics devices, the converter module temperature can be reduced, leading to a decrease in the overall IMD temperature.

2.2 WBG topologies for motor-drives

2.2.1 Problems in Voltage Source Inverter with WBG

Typical motor drives predominantly use a two-level, three-phase voltage source inverter (VSI) topology due to its high efficiency, simple control requirements, and low cost. As illustrated in Figure 2.1, a three-phase VSI consists of three commutation cells with two transistors each, forming three switched voltage nodes. In each leg, the top and bottom switches operate complementarily, ensuring they are never switched on simultaneously.

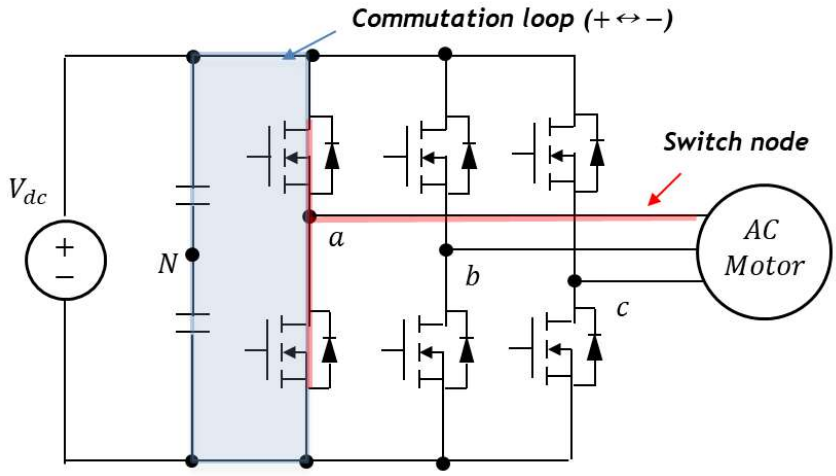


Figure 2. 1. Typical circuit diagram in 3-φ VSIs. Commutation loops (blue) and switch nodes (red) of VSIs.

The VSI operates by chopping the DC voltage of the DC-link capacitor to generate the required load voltage. The Root-Mean-Square (RMS) output voltage is applied to the load using the fixed DC voltage and pulse time. The square-form output voltage is generated by controlling the turn-on time of the top switch of each leg, comparing the triangular carrier frequency (Vc) with the required command voltages (V_{ma}, V_{mb}, V_{mc}), as shown in Figure 2.2. The voltage at each switching node has a magnitude of ±Vdc/2 based on the neutral point of the DC link capacitor.

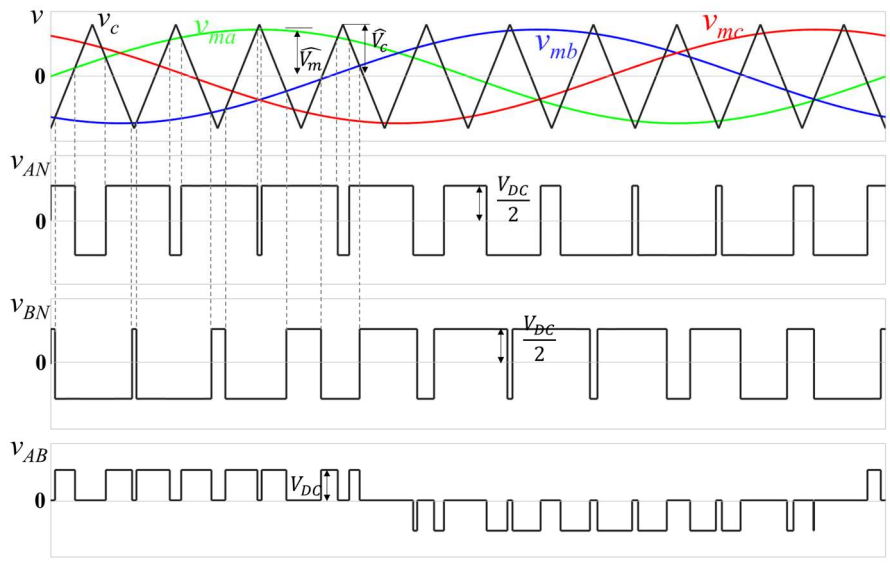


Figure 2. 2. Typical output voltage waveform of VSis [40]

However, the generated voltage has a high dv/dt, which can cause issues due to parasitic components in the interconnections of all power semiconductors. These parasitic components lead to higher dv/dt if the switching frequency increases. In the case of WBG power semiconductors with low switching loss, increasing the switching frequency should be considered to maximize their advantages. However, previous studies have shown that a switching frequency of 50 kHz or more and dv/dt of over 10 V/ns require consideration of short cable lengths. The long connection cable with high switching frequency can lead to overvoltage problems in the motor, potentially damaging motor insulation and reducing insulation life, as shown in Figures 2.3(a) and 2.3(b) [41-42].

CM EMI, measured based on the length of the connection cable (Figure 2.4), increases with cable length, significantly boosting CM EMI in the frequency range below 5 MHz. This can affect bearing life, as bearings have the highest failure rate in electromechanical systems. With the advent of IGBTs, the issue of bearing current has become more prominent, and this problem could become even more severe with WBG-based drives. The inverter can induce various types of bearing current, with electric discharge machining, circulating bearing currents, and rotor ground currents being the most harmful. Pitting, frosting, and fluting are some of the effects caused by bearing currents (Figure 2.5) [41].

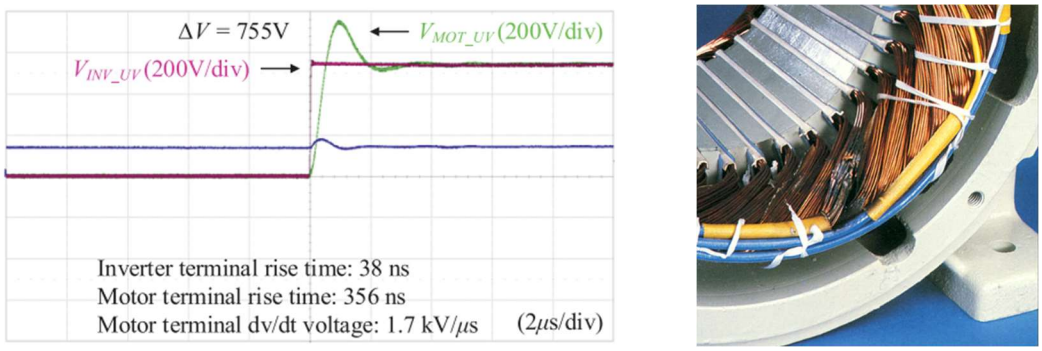


Figure 2. 3. (a) Over voltage of motor terminal with 3 m cable [43], (b) Motor winding damaged by voltage surge [44]

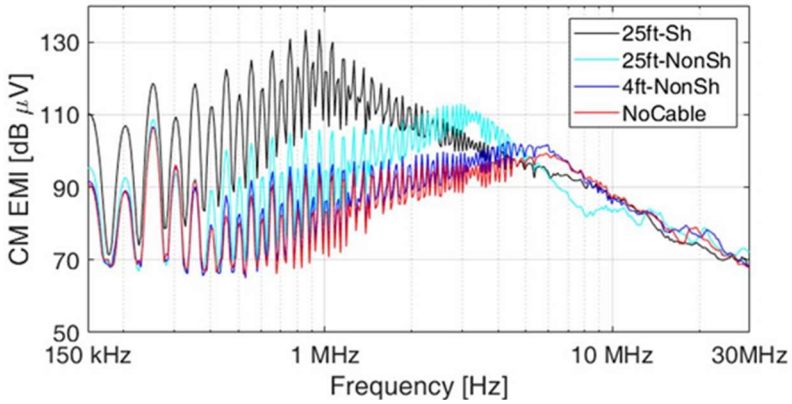


Figure 2. 4. Measured conducted CM EMI from the LISN of the VSI for the four cable configurations [41]

Additionally, VSI requires protection circuits against motor short circuits and line-to-line shorts. Compared to IGBTs or Si MOSFETs, SiC MOSFETs are more vulnerable to short circuits, necessitating protection measures. The temperature rise in SiC-MOSFETs is 15~20 times larger than in Si-IGBTs at the short circuit [45-48].

These various issues have been reported by multiple researchers as problems that arise when increasing the switching frequency in traditional VSIs using WBG semiconductors. Figure 2.6 summarizes these problems and lists potential solutions.

However, nearly all methods dilute the desired advantages of introducing WBG devices into motor drives. Increased weight, size, switch count, inverter cost, loss, and complexity are not favorable for general motor drive applications.

Figure 2. 5. Bearing exposed to bearing current. Bearing race track damaged due to EDM current [49]

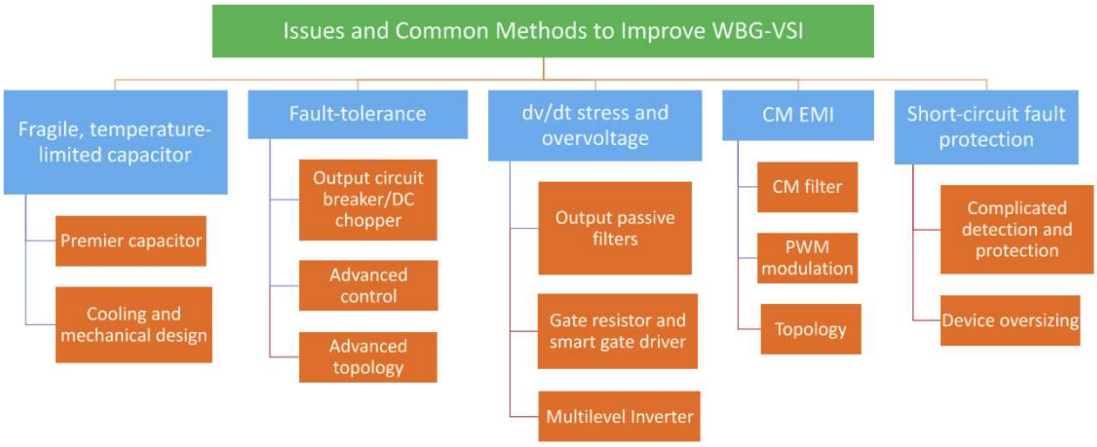


Figure 2. 6. Problems caused by drop-in replacement of WBG switches in VSIs [18]

2.2.2 Boost-Voltage Source Inverter with EMI filter

To address the fundamental issue of high dv/dt, one of the most basic methods to consider is the use of an LC filter, as shown in Figure 2.7. By adding inductors and capacitors, which serve as EMI filters, between the motor and the inverter, improvements can be achieved by reducing the high dv/dt.

In Figure 2.8(a), the red waveform represents the output voltage of a two-level VSI, which can be converted to a green sinusoidal voltage using an LC filter, commonly referred to as a sine filter. The blue line indicates the motor current in this configuration. As illustrated in Figure 2.8(b), this sine filter significantly helps in reducing CM EMI. The

blue graph, which represents the filtered EMI, is smaller in most areas compared to the without filter.

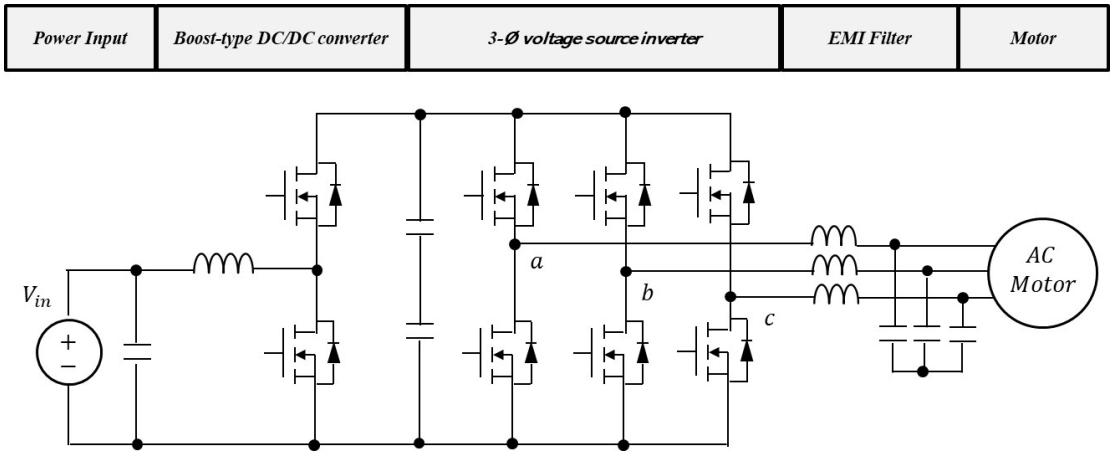
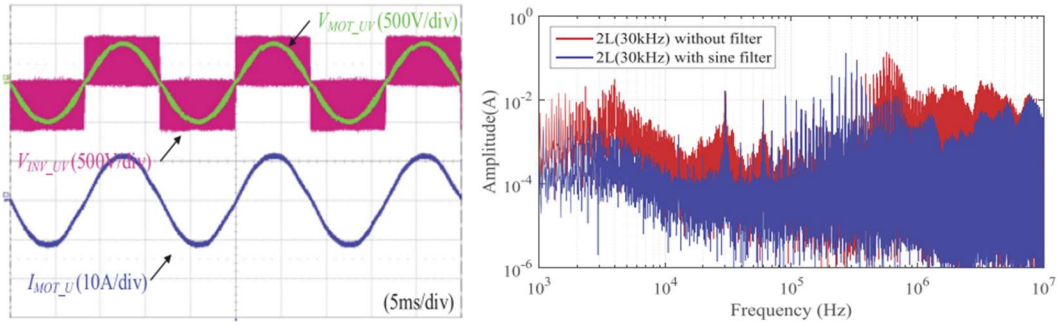


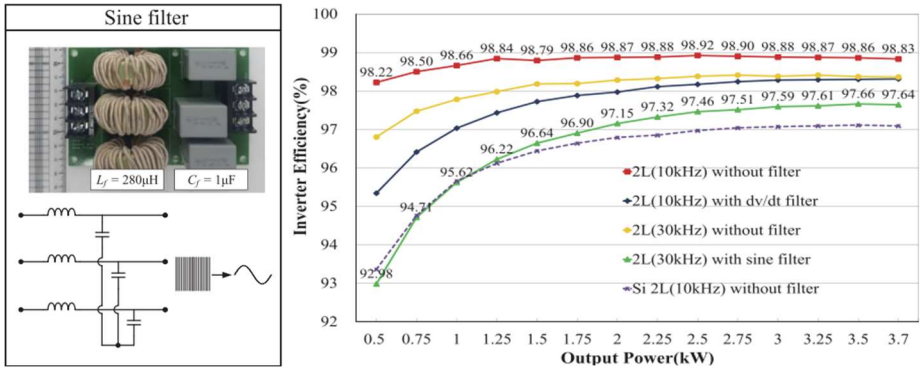
Figure 2. 7. Boost-Voltage Source Inverter with EMI Filter



(a) (b)

Figure 2. 8. VSI with LC Filter; (a) Voltage and current waveform, (b) comparison 2L-VSI common mode current spectrum between without or with sine filter [50]

However, as shown in Figure 2.9(a), the addition of an LC filter requires extra passive components, which increases the overall system volume. Furthermore, as illustrated in Figure 2.9(b), these additional passive components also introduce extra losses, thereby reducing the inverter's efficiency. When comparing the yellow graph (without the filter) and the green graph (with the filter) at the same frequency of 30kHz, a significant drop in efficiency is observed.



(a) (b)

Figure 2. 9. Configuration of Sine Filter (a) and comparison of the measured efficiency data of inverter without and with filters (b) [50]

Finally, in traditional VSIs, the output voltage is generated using the input DC voltage. Since the output voltage cannot exceed the input voltage, if a higher motor voltage is required, either field weakening control or an additional DC/DC boost circuit must be added. This boost converter-based configuration necessitates at least two additional power switches with a DC inductor and still requires a large DC link capacitor, which has limitations for high-temperature operation, as seen in Figure 2.7.

2.2.3 Buck-Current Source Inverter

The operating temperature limitation of the DC link capacitor discussed in Section 2.2.1, along with the additional LC filter requirements, has led to renewed interest in current source inverters (CSIs), which were primarily considered for high-power inverters in the past. The bulky DC link capacitor, which has the highest failure rate and temperature limitations in power electronics, can be replaced with a more rugged and high-temperature-operating inductor in CSIs [51].

As shown in Figure 2.10, since the CSI requires a current source, a buck converter with a DC link inductor is needed to control the DC current to the CSI when the input is a DC

voltage. These DC link inductors generally have higher operating temperatures and lower failure rates compared to DC link capacitors.

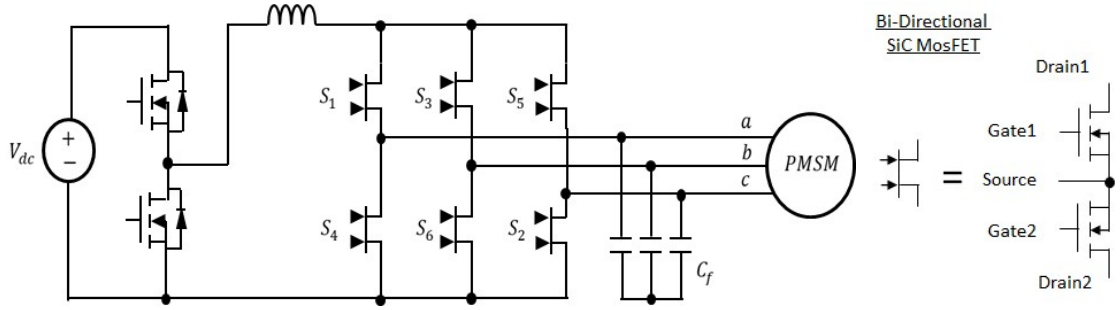
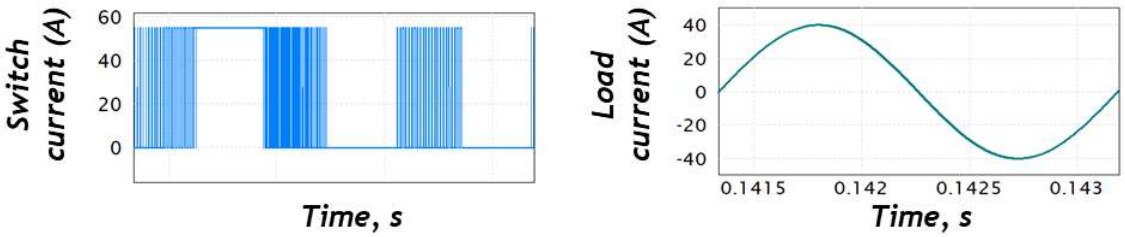


Figure 2. 10. Circuit schematic of Buck CSI-fed PMSM using Wide-Band-Gap Bi-directional Switches and schematic of MOSFET BDS in common source configuration

Furthermore, the CSI chops the generated DC current using six bidirectional switches, in Figure 2.10, as illustrated in Figure 2.11(a), to produce a load current waveform as shown in Figure 2.11(b). This results in a switching current with a high di/dt. The output filter capacitor shapes this high di/dt current into sinusoidal voltages and currents that are delivered to the load [7,51-53].

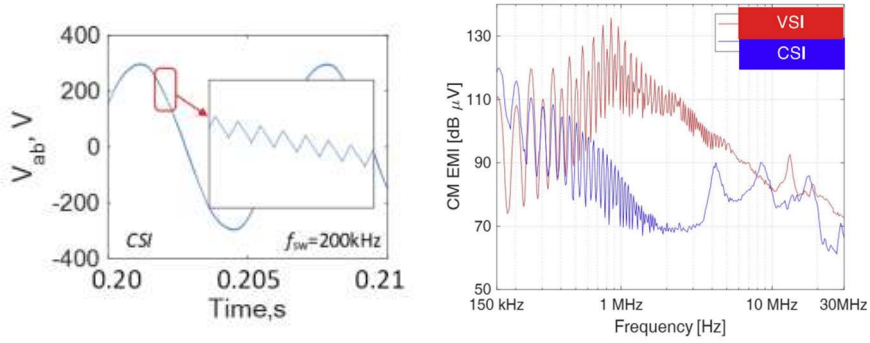


(a) (b)

Figure 2. 11. The simulation result of the three-phase CSI: (a) the power switch current, (b) the load current

Due to the high switching frequency of WBG semiconductors, the filter capacitor can be miniaturized, allowing the use of film capacitors or very compact Multilayer Ceramic Capacitors (MLCCs) that are suitable for high-temperature operation.

Additionally, as shown in Figure 2.12(a), this filter capacitor allows the generation of a load voltage with very low dv/dt, close to the sinusoidal waveform. Consequently, as depicted in Figure 2.12(b), the overall CM EMI characteristics are significantly lower compared to traditional VSIs, represented by the red graph.



(a) (b)

Figure 2. 12. The load voltage of CSI with low dv/dt (a) and the Common-mode EMI spectrum of CSI (b) [54]

Finally, another advantage that CSI can offer over traditional VSI in motor drives is CSI's natural voltage boost function. In CSI, space vector modulation is required, during which DC current can be freewheeling to form a zero current vector. This allows the DC inductor current to increase, and when the active current vector is provided to the motor, the filter capacitor can be charged, thereby increasing the voltage that can be applied to the motor. In Table 2.2, comparing the left and right sections shows that the line-to-line voltage increases with the boosting function, resulting in improved drive efficiency compared to when field weakening control is used [55].

Table 2. 2. Comparison of control algorithms for CSI motor drive systems without boosting and with boosting, using optimal modulation index and current angle. [55]

Speed [rpm]	*m*	*γ* [degree]	Peak line-line voltage [V]	Power factor	Drive Sys. Effic. [%]	Speed [rpm]	*m*	*γ* [degree]	Peak line-line voltage [V]	Power factor	Drive Sys. Effic. [%]
Original modulation index (m = 1)						*Optimal modulation index and current angle*					
3,200	1	0	710.9	0.785	94.68	3,200	1	0	710.9	0.785	94.68
4,000	1	38.66	568.6	0.926	94.57	4,000	0.845	12.80	803.2	0.812	96.14
8,000	1	67.28	527.9	0.997	94.49	8,000	0.565	41.60	985.8	0.978	97.17
12,000	1	75.10	527.7	0.999	94.47	12,000	0.683	65.98	979.5	0.807	96.60
16,000	1	78.84	531.3	0.989	94.46	16,000	0.775	74.49	995.5	0.712	96.12
20,000	1	81.13	538.0	0.979	94.44	20,000	0.835	78.63	996.0	0.662	95.75

2.2.4 Buck-Boost Y-Inverter

As discussed in Section 2.2.3, the CSI provides a boosting function where the output voltage exceeds the input voltage. However, the control aspect is more complicated and has limitations on its boost ratio. In contrast, the Y-Inverter inherently includes a step-up converter, allowing for an easily controllable boosting voltage. This makes it a more efficient topology for motor drive systems using batteries or fuel cells with significant variations in input voltage [56-58].

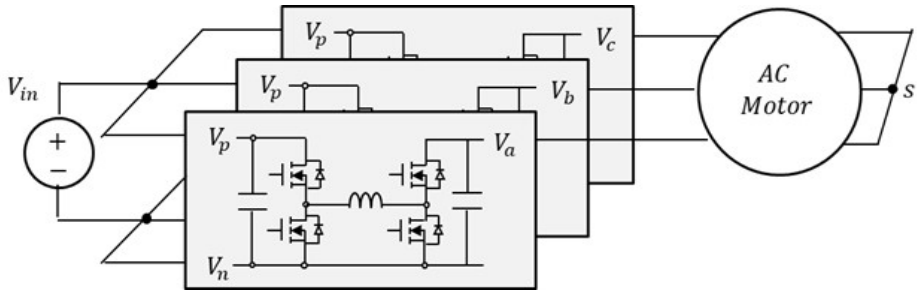


Figure 2. 13. Buck-Boost Y-inverter topology for the three-phase motor drives

The Buck-Boost Y-Inverter motor drive, which leverages these strengths, consists of three identical, non-isolated four-switch buck-boost DC/DC converters connected to a common star (Y) point, as shown in Figure 2.13. This configuration allows flexibility in voltage conversion, enabling the AC output voltage to be either higher or lower than the DC input voltage. Additionally, the Y-VSI includes an integrated LC output filter, producing continuous and sinusoidal motor voltages with lower dv/dt, eliminating the need for additional filters between the inverter and the motor.

In operation, when a higher voltage than the input is needed, the top left switch is turned on, using the right-side boost-leg to generate an AC voltage greater than the input voltage. Conversely, when a lower voltage than the input is needed, the top right switch is turned on, using the left-side buck-leg to generate an AC voltage lower than the input voltage. This results in an AC voltage with a DC offset at the output capacitor, which cancels out at the three-phase motor terminals, producing a near-sinusoidal wave.

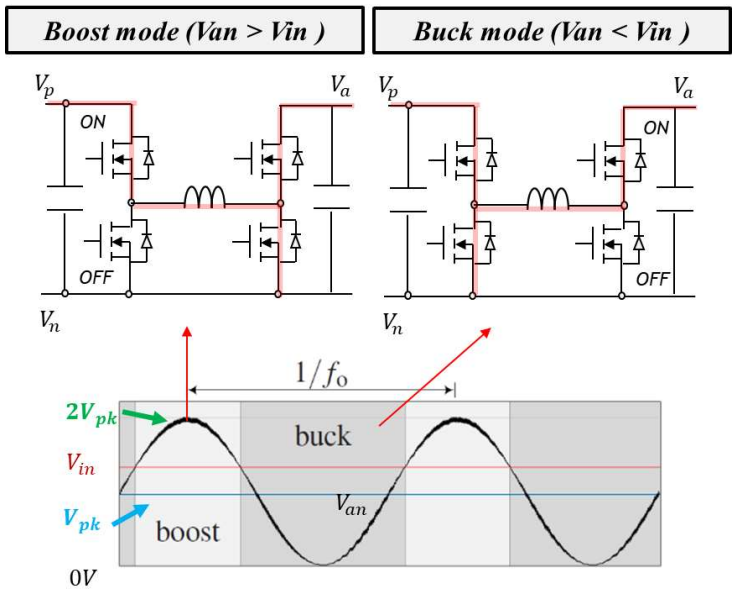


Figure 2. 14. Illustration of the principle of operation of the Y-inverter [59].

Due to the boost converter, the magnitude of the voltage output from the inverter is theoretically unlimited, allowing high-speed rotation of the PM motor without the need for field weakening control. Increasing the motor voltage reduces the motor current for the same torque or increases the motor's power density by increasing the number of motor poles.

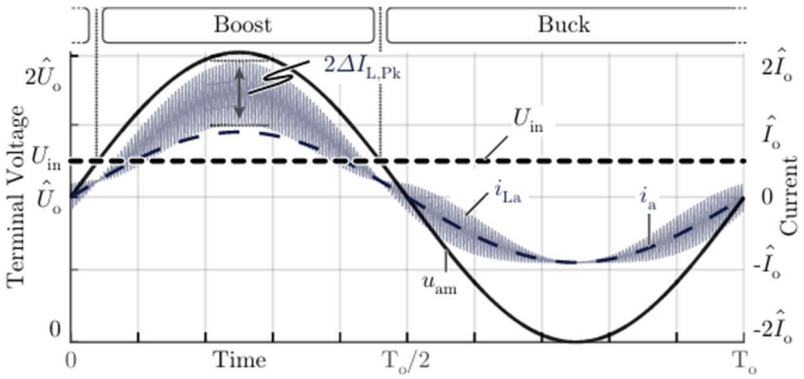


Figure 2. 15. Operating principle of a Y-inverter. The generated voltage and current waveforms of phase-leg are depicted, along with the resulting sinusoidal motor currents and voltages, and the DC-inductor currents [57].

The buck leg can use power semiconductors with lower blocking voltage and lower inductor current ripple, such as Si-MOSFETs. This Si-SiC hybrid structure can provide cost advantages in the Y-Inverter design [60].

However, as shown in Figure 2.15, the inductor current ripple in the DC/DC converter increases in boost mode, necessitating the use of high-speed switching WBG power semiconductors for the boost leg.

2.2.5 Summary

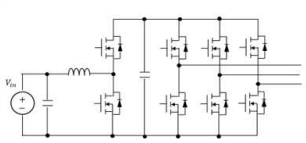
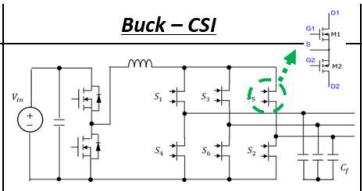
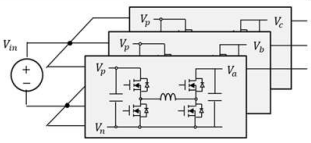
	Boost - VSI	Buck – CSI	Y-Inverter
			
# of Switches	Total 8 (2 + 6)	Total 14 (2 + 6 x 2)	Total 12 (6 + 6)
# of Passive component	1 Inductor, 1 input Capacitor, 1 DC-link Cap. + (3 Inductor and 3 Filter Cap.)	1 Inductor, 1 DC-link Cap., 3 Filter Cap.	3 Inductor, 1 input Cap., 3 Filter Cap.
Strength	# of switches	Sinusoidal output voltage Small number of passives	Sinusoidal output voltage, Si-SiC hybrid configuration
Drawback	EMI filters lead to additional losses	Needs current source	High inductor ripple current (@ boost mode)

Figure 2. 16. Comparison of WBG topologies for motor drives

Figure 2.16 summarizes a comparison of three possible topologies using WBG switches. The comparison considers the number of power switches and passive components, as well as the advantages and disadvantages of each topology. Topologies with step-up functionality, allowing the output voltage to exceed the input voltage, are also considered to minimize field weakening control during high-speed rotation.

The Boost-VSI requires the fewest power switches among the topologies. However, due to its high dv/dt, it necessitates output EMI filters with numerous passive components. This requirement impacts the large volume and lower efficiency from LC filters, making Boost-VSI less favorable despite its simplicity. Additionally, considering the boost functionality,

the topology uses the fewest number of power switches, but the blocking voltage specification of all the switches must be increased.

Both the CSI and Y-inverter require a large number of power switches, 14 and 12, respectively. However, they require fewer passive components and do not need additional output filters due to their low dv/dt. In a CSI, a buck converter is required for DC current control, whereas in a Y-inverter, careful design of the inductors and switches is necessary due to the increased current ripple during voltage boosting.

As shown in Figure 2.17, studies on 1kW-class DC/AC inverters indicate that the Buck-CSI generally has the best electrical efficiency [57]. Of course, depending on the rated power and the magnitude of the input voltage, parallel connection of DC/DC converters in Buck-CSI or Boost-VSI could be required. Therefore, preferences may vary depending on the application. Since this research aims to increase power density through new power packaging designs, we will focus on the Buck-CSI, which has the fewest passive components and the highest efficiency.

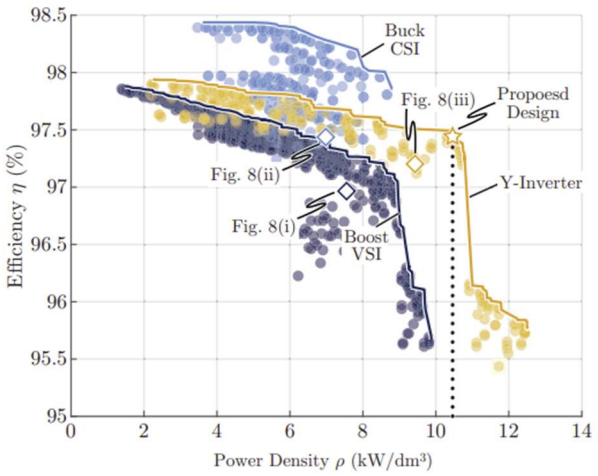


Figure 2. 17. Comparison of the efficiency with power density for WBG topologies [57]

However, additional research was conducted on the Y-Inverter, specifically aimed at low-voltage electric vehicles. This work is briefly summarized in Appendix D.

3. Three-phase Current Source Inverter

In this chapter, we analyze the basic operation of the three-phase Current Source Inverter (CSI), selected in Chapter 2 after comparing various Wide Bandgap (WBG) topologies. The CSI requires unique switching operations compared to the conventional Voltage Source Inverter (VSI).

Firstly, unlike the VSI, the CSI requires power switches with bidirectional blocking voltage capabilities. We will compare the different types of such switches and analyze high-efficiency power switch configurations to enhance power density.

Additionally, the CSI, unlike the VSI, requires a continuous current conduction path. This necessitates the simultaneous control of at least two power switches, typically utilizing unique switching patterns based on Space Current Vector Modulation. We will analyze these switching patterns and evaluate the voltage and current stresses on the power switches.

Based on this analysis, simulations will be conducted to examine the requirements for implementing structurally and functionally integrated motor drives.

3.1 Principle of Operation

3.1.1 Current-Voltage characteristics

The current-voltage characteristics of the power semiconductor required in CSI differ significantly from those of VSI. In general, VSI, unipolar block voltage, and bipolar current conduction characteristics are required. Therefore, a single MOSFET or IGBT with an anti-parallel diode is usually used. On the other hand, in CSI, a reverse blocking switch capable of blocking both polarities voltages is required. Then, the switch's current requires a unidirectional current, as shown in Figure 3.1 [61].

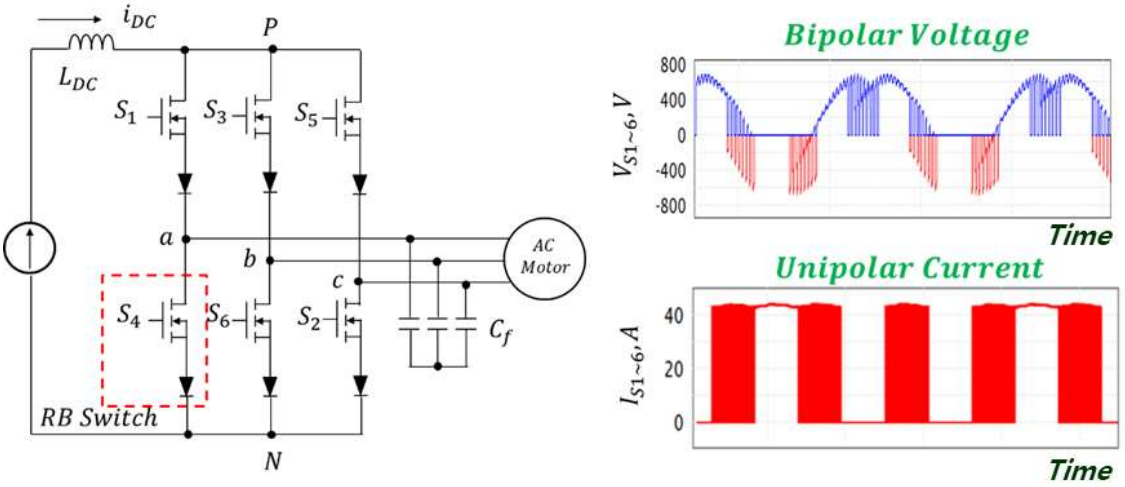
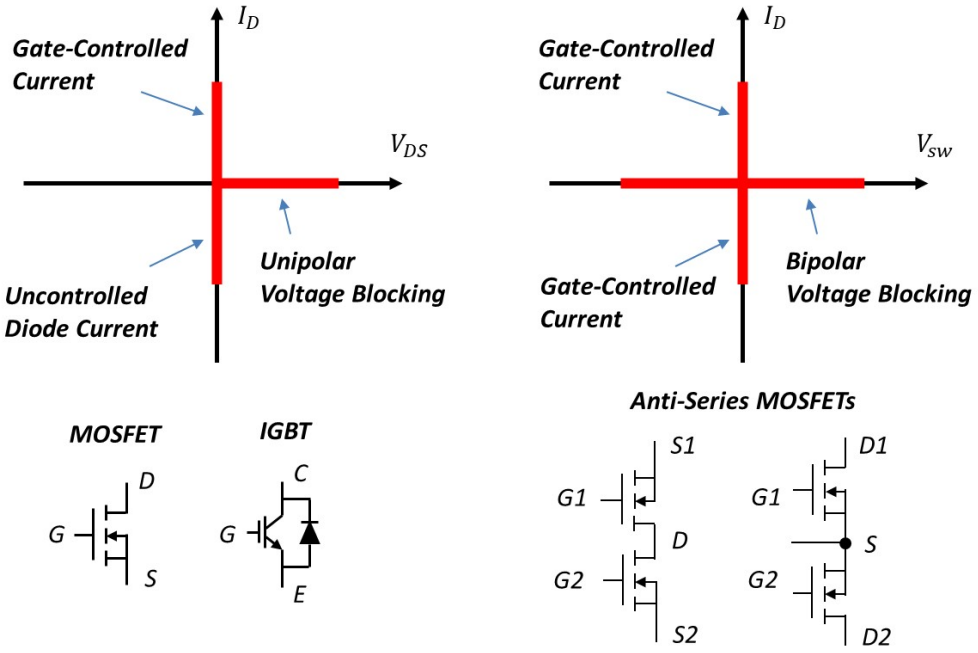


Figure 3. 1. 3-Ø Current Source Inverter with Reverse-voltage-blocking (RB) switches.

This "FET+Diode" configuration readily meets this requirement. However, the CSI with RB switches suffers an efficiency penalty due to the voltage drops across the series-connected diodes [62]. Therefore, to improve the efficiency of CSIs, the "FET+FET" bidirectional (BD) configuration is considered, conducting current in both polarities. It makes more appealing candidates for use in CSIs.

To reduce conduction losses, CSIs require the design of bidirectional switches. Figure 3.2(a) shows that conventional power switches block unipolar (forward) voltage and

operate as diodes under reverse voltage. However, bidirectional switches require blocking both forward and reverse voltages and controlling current in both directions. For this reason, a structure using two MOSFETs is typically considered. As you can see in Figure 3.2(b), bi-directional switches can be implemented with discrete devices using anti-series combinations of conventional forward-blocking switches [18,62].



(a) Conventional Forward-Blocking Switches (b) Bi-directional Switches

Figure 3. 2. Power Semiconductor Switch Classes

3.1.2 Bi-directional switch

The bidirectional switch can typically have two configurations: a “common-drain” structure and a “common-source” structure.

WBG devices are designed as lateral MOS-gated devices, which are typical for gallium nitride devices. Their symmetrical channels make them good candidates for monolithic bi-directional switches. The HEMT (High Electron Mobility Transistor) structure is similar to Si-based MOSFETs, which is also reflected in their voltage-current characteristics. Therefore, the lateral structure of HEMTs offers an advantage because it does not contain a body diode, making it an excellent candidate for a monolithic bidirectional switch.

Consequently, as shown in Figure 3.3, a monolithic switch can be designed with a common drain, sharing the drift region to create a bidirectional switch. This design can reduce the on-resistance [56].

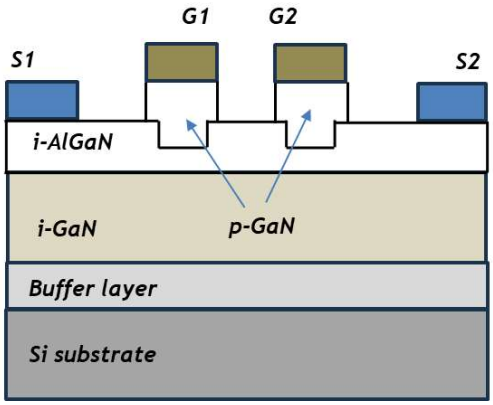


Figure 3. 3. Internal device structure of the monolithic bidirectional switch based on the GaN-HEMT

However, while monolithic bidirectional switches are being researched at the prototype stage, there have yet to be commercially available devices on the market. Additionally, GaN HEMTs with lateral structures are suitable for monolithic bidirectional switch design but have limitations in blocking voltage. Applications requiring over 600V need MOSFETs with vertical structures, making monolithic configurations challenging. Furthermore, as explained in Chapter 2, SiC exhibits better thermal conductivity than GaN, making it more

suitable for high-temperature operations and thus more appropriate for IMD design. Therefore, this study focuses on research using SiC MOSFET.

Due to the difficulty of monolithic design with SiC because of its vertical structure, as seen in Figure 3.4, bidirectional switch fabrication can realistically be achieved using two commercial unipolar power switches connected via a Printed Circuit Board (PCB) or power module packaging. The latter approach is more suitable for increasing power density. Given the temperature limitations of commercially available power switches, this study aims to achieve physical integration through research based on power packaging.

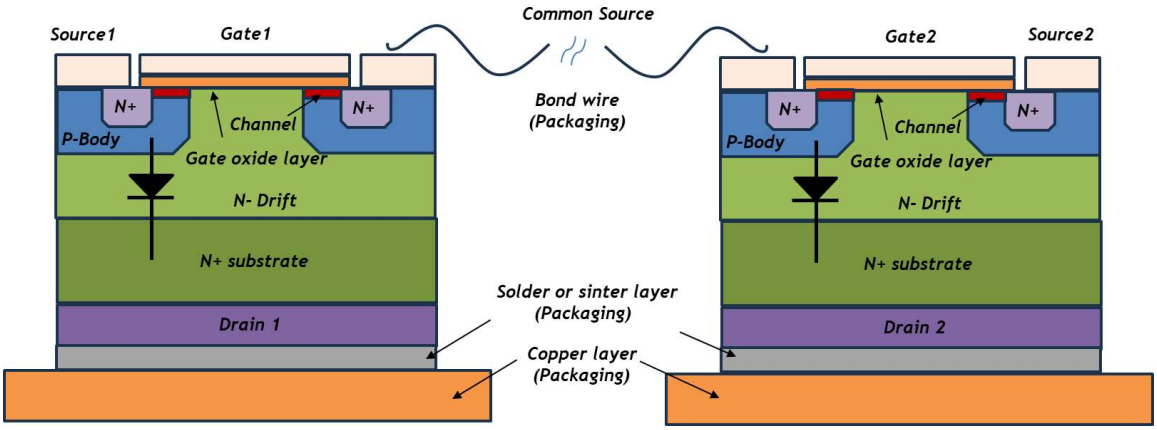


Figure 3. 4. Example of simplified a common-source bidirectional switch configuration using vertical structure MOSFETs

When configuring the three-phase CSI using the common-drain structure, one source pin of the bidirectional switch is connected to either the positive or negative switch node of the DC input. This reduces the number of isolated converters required for the gate drive circuit, allowing the use of a total of five isolated converters [56,63].

However, this configuration is challenging for separate testing of the independent discrete BDS and offers less design flexibility. Therefore, this study primarily considers the design of bidirectional switches with the common-source structure. Although this increases the number of isolated converters to six, it enhances the design flexibility of the system.

3.1.3 Space Vector Modulation

The three-phase Current Source Inverter (CSI) topology with six "common-source" current-bi-directional switches is depicted in Figure 3.5. It is assumed that in steady-state operation, this voltage source consistently provides the voltage required to sustain the average DC-link current (i_{DC}) at the design-specified value.

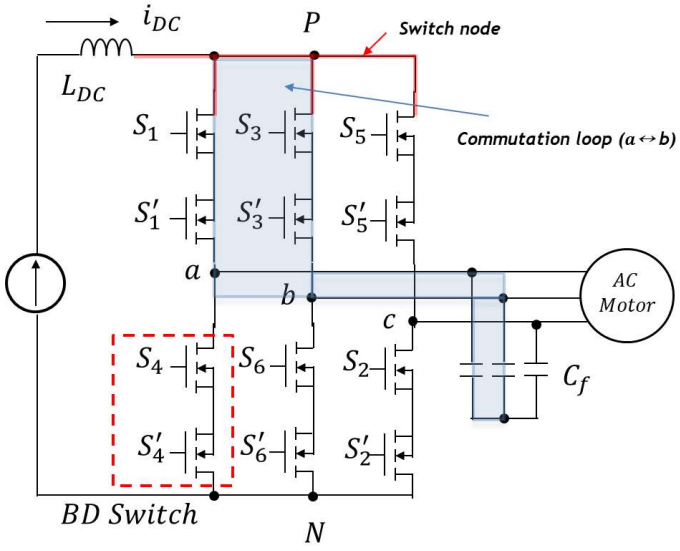


Figure 3. 5. 3-Ø Current Source Inverter with bi-directional (BD) switches: Commutation loops (blue) and switch nodes (red) of CSIs.

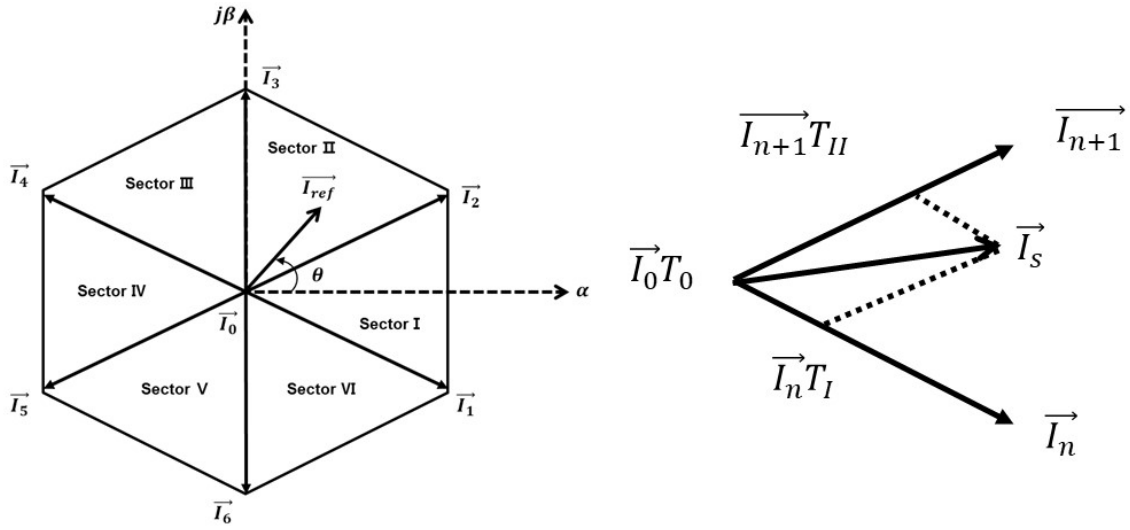
Space Vector Modulation (SVM) is the most commonly used strategy in three-phase Current Source Inverters (CSIs). This strategy offers low switching losses because it utilizes a constant DC link current and performs three commutation processes per PWM period.

Such switch operations are required to generate a demanded current and transmit the generated current to a load. Therefore, first, a method for generating a three-phase current using a switch combination will be described. In Table 3.1, CSIs have six active vectors and three zero vectors, and two switches must be operated in pairs to output them [64].

As shown in Figure 3.6 (a), when operating CSI by SVPWM, the output current vector ($\overrightarrow{I_{ref}}$) is divided into six sectors. A reference-current vector ($\overrightarrow{I_s}$) can be output by combining two active vectors ($\overrightarrow{I_n}, \overrightarrow{I_{n+1}}$) and one zero vector ($\overrightarrow{I_0}$) for each vector, Figure 3.6 (b). Each active vector has a magnitude of a DC Link current, and if the DC-current may be controlled according to a target current, an optimized current vector may be output.

Table 3. 1. Switching state in CSIs and corresponding phase switching functions and switching space vectors

Three Zero Current Vectors					Six Active Current Vectors				
Vector	On Switches	$\overrightarrow{\iota_a}$	$\overrightarrow{\iota_b}$	$\overrightarrow{\iota_c}$	Vector	On Switches	$\overrightarrow{\iota_a}$	$\overrightarrow{\iota_b}$	$\overrightarrow{\iota_c}$
$\overrightarrow{I_0}$	S1, S4	0	0	0	$\overrightarrow{I_1}$	S6, S1	i_{DC}	$-i_{DC}$	0
$\overrightarrow{I_0}$	S2, S5	0	0	0	$\overrightarrow{I_2}$	S1, S2	i_{DC}	0	$-i_{DC}$
$\overrightarrow{I_0}$	S3, S6	0	0	0	$\overrightarrow{I_3}$	S2, S3	0	i_{DC}	$-i_{DC}$
					$\overrightarrow{I_4}$	S3, S4	$-i_{DC}$	i_{DC}	0
					$\overrightarrow{I_5}$	S4, S5	$-i_{DC}$	0	i_{DC}
					$\overrightarrow{I_6}$	S5, S6	0	$-i_{DC}$	i_{DC}



(a) (b)

Figure 3. 6. Current Space Vector modulation of 3-Ø Current Source Inverter

The product of the current space vector ($\overrightarrow{I_n}, \overrightarrow{I_{n+1}}, \overrightarrow{I_0}$) and switching time ($T_0,\ T_I,\ T_{II}$) is equated with the sum of the products of corresponding. The dwell time can be calculated with space vectors, and corresponding time intervals follow, where n is the number of the active vector. ($1 \leq n \leq 6$):

$$\overrightarrow{I_s}T_s = \overrightarrow{I_n}T_I + \overrightarrow{I_{n+1}}T_{II} + \overrightarrow{I_0}T_0 \tag{3.1}$$

$$T_s = T_I + T_{II} + T_0 \tag{3.2}$$

T_s is the total switching time. It's same to the control time. The magnitude of the output current can be calculated as a ratio using the dc-link current. This is called the modulation index (m_a) and I_s^* is the desired current in Eq. (3.3).

$$m_a = \frac{I_s^*}{I_{dc}},\quad 0 \leq m_a \leq 1 \tag{3.3}$$

Based on the m_a, dwell times of active current vectors (T_I, T_{II}) can be calculated as like (3.4) and (3.5). Here, the k is the sector number ($1 \leq k \leq 6$).

$$T_I = m_a \sin\left(\frac{\pi}{6} - \left(\theta - \frac{(k-1)\pi}{3}\right)\right)T_s \tag{3.4}$$

$$T_{II} = m_a \sin\left(\frac{\pi}{6} + \left(\theta - \frac{(k-1)\pi}{3}\right)\right)T_s \tag{3.5}$$

The total of switching or control time (T_S) is constant. Therefore, the zero vector dwell time (T_0) can be determined as follows:

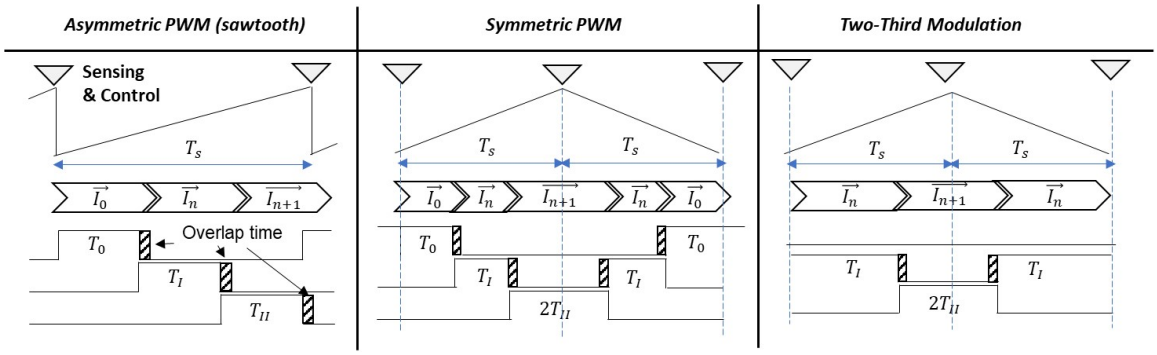
$$T_0 = T_s - T_I - T_{II} \tag{3.6}$$

3.1.4 Switching sequence

In order to output the active vector and the zero vector, explained in (3.1.3), a sequence with a specific order must be created, as shown in Figure 3.7. CSIs need to generate a specific switching sequence to implement SVPWM, and the losses and quality of output current may change according to the number and order of the sequences. Usually, five or seven sequences are used, as seen in Table 3.2, but it can be seen that it is advantageous to have five switching sequences in terms of switching loss throughout the study [65].

Table 3. 2. The state sequences

Modulation	State Sequence	Note
Asymmetric PWM	$[\overrightarrow{I_0}]\,[\overrightarrow{I_n}]\,[\overrightarrow{I_{n+1}}]$	CW-asymmetric pwm
	$[\overrightarrow{I_0}]\,[\overrightarrow{I_{n+1}}]\,[\overrightarrow{I_n}]$	CCW-asymmetric pwm
Symmetric PWM	$[\overrightarrow{I_n}]\,[\overrightarrow{I_0}]\,[\overrightarrow{I_{n+1}}]\,[\overrightarrow{I_0}]\,[\overrightarrow{I_n}]$	Zero Vector-symmetric pwm
	$[\overrightarrow{I_0}]\,[\overrightarrow{I_n}]\,[\overrightarrow{I_{n+1}}]\,[\overrightarrow{I_n}]\,[\overrightarrow{I_0}]$	In Vector-symmetric pwm
	$[\overrightarrow{I_0}]\,[\overrightarrow{I_{n+1}}]\,[\overrightarrow{I_n}]\,[\overrightarrow{I_{n+1}}]\,[\overrightarrow{I_0}]$	In+1 Vector-symmetric pwm
TTM	$[\overrightarrow{I_n}]\,[\overrightarrow{I_{n+1}}]$	without zero current vector



(a) (b) (c)

Figure 3. 7. (a) shows the features of characteristic of Asymmetric PWM and (b) is indicated features of Symmetric PWM (c) is presented the characteristic of Two-Third Modulation.

Besides, according to a recent study [66], the six methods in Table 3.2 were discussed, and it can be seen that 8% of conduction loss and 86% of switching loss can be reduced when Two-Third Modulation (TTM) is applied according to the modulation index. However, a DC-DC converter and synergetic control are required in this method.

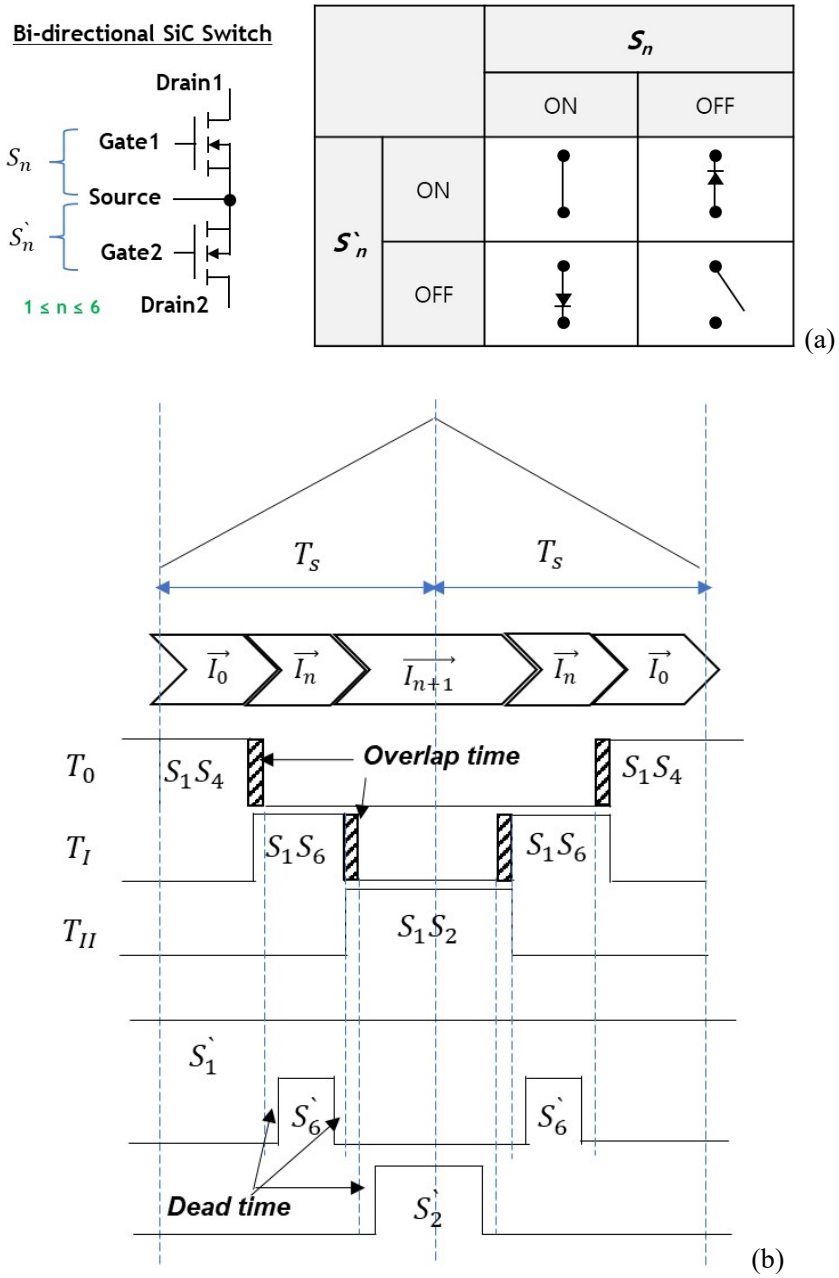


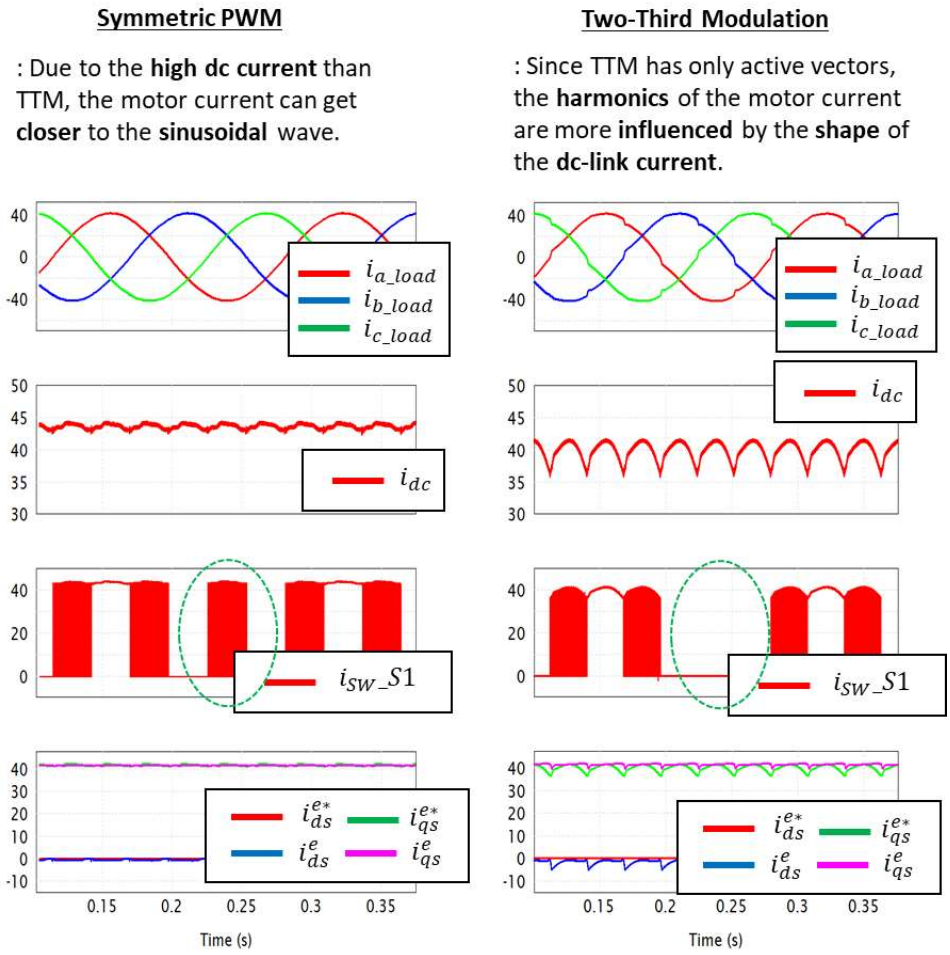
Figure 3. 8. (a) Bi-directional switch configuration and the switch function corresponding to the gate signal, (b) example of the switching sequence with the overlap time and the dead time at Sector I.

A bidirectional switch could be configured using two MOSFETs, as shown in left Figure 3.8 (a), and depending on the gate-source voltage of each power semiconductor (i.e., MOSFET), it can be operated in four states as shown in the table on the right of Figure 3.8(a). For example, if both MOSFETs apply 0V or a negative bias voltage to the gate voltage, the power semiconductor is in an open circuit state. That is, it becomes possible to block the reverse voltage in both polarities. If a gate voltage is applied to the upper MOSFET, the upper power semiconductor is conducted to allow current to be conducted from top to bottom. The lower power semiconductor allows current to flow in one direction through the body diode. Conversely, if a gate voltage is applied to the lower power semiconductor, the current should flow in reverse. If the gate voltage is applied to both power semiconductors above the threshold voltage, current can flow to both sides.

Practical bidirectional (BD) switches have finite switching speeds. As a result, overlapping time is required during commutations to ensure the existence of a current path for the DC-link inductor at all times and prevent transient overvoltage. However, BD switches that are fully gated on to conduct current in both polarities create the risk of dangerously interphase short-circuit current pulses whenever the BD switches in two adjacent phases are transiently on at the same time [67-69, 71]. Therefore, a switching sequence using a body diode is required in the energy phase-to-phase commutation. Of course, the body diode is very helpful in preventing the short-circuit between phases but causes a large conduction loss. Therefore, as can be seen in Figure 3.8 (b), the lower power semiconductor is turned on in consideration of sufficient dead time to minimize conduction loss, thereby increasing the efficiency of the inverter.

3.2 Simulation Model

In Figure 3.9, the performance of the CSI-fed PMSM was verified through the simulation model using PSIM, employing both Symmetric PWM and Two-Third PWM techniques.



(a) (b)

Figure 3. 9. The results of the simulation model (a) is shown that features of control characteristic of Symmetric PWM and (b) indicate control features of Two-Third Modulation at 6 Hz electrical frequency.

Symmetric PWM and TTM can be designed to facilitate sampling and control operations twice within one cycle period. Additionally, since the switching operation of a power semiconductor can affect the precision of current and voltage sensing—which is crucial for maintaining control stability in practical applications—symmetric PWM and TTM are

more suitable for implementing high-speed machines in practice. Asymmetric PWM, on the other hand, must find ways to mitigate switching noise.

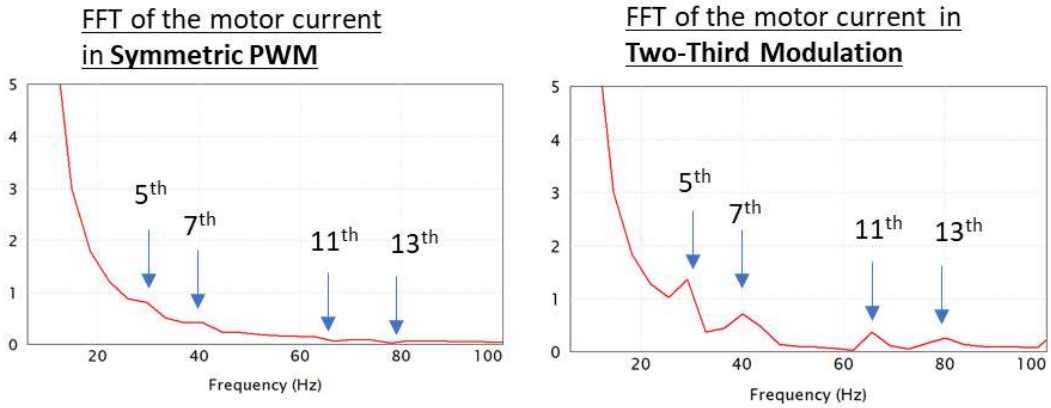


Figure 3. 10. The FFT results of the simulation (a) is shown that features of control characteristic of Symmetric PWM and (b) is indicated control features of Two-Third Modulation.

Table 3. 3. The simulation results of the harmonics distortion depending on the PWM method.

$I_n/I_1(\%)$	5^{th}	7^{th}	11^{th}	13^{th}
PWM	1.95	0.93	0.23	0.10
TTM	3.43	1.78	0.90	0.65
	+1.5%	**+0.9%**	**+0.7%**	**+0.6%**

In general, the CSI requires a power converter capable of controlling the DC-link current to prevent overcurrent and damage from switch failures. Consequently, the DC-link current in the CSI can be managed using a power converter in conjunction with the PWM method. Due to the existence of a zero current vector in symmetric PWM, the maximum modulation index is limited when controlling the DC-link current through the power converter. Therefore, the controlled DC-link current by the power converter must be higher than the desired output current of the CSI. In contrast, TTM allows the controlled DC-link current to be close to the desired output current of the CSI since it only needs to generate the active current vector.

This result also shows that the control of the DC-DC converter varies depending on whether symmetric PWM or TTM methods are used. Although both methods yield the same inverter output current under identical load conditions, TTM necessitates the control of the DC-link current to eliminate the zero current vector. The harmonic content of the current increases with the shape of the DC current, as shown in Figure 3.10, necessitating careful control of the DC current in TTM. Conversely, for symmetric PWM, the DC-link current should be maintained at a constant level, with the modulation margin required by the CSI ensuring higher current control compared to TTM. Consequently, the losses in the power converter may be greater than in TTM. However, since symmetric PWM controls the DC current in a constant form, its output current harmonics are lower than those of TTM. More detailed data are provided in Table 3.3, particularly noting the increase in 5th-order harmonics [70]. As indicated in previous studies [66], syngeneic control between the CSI and DC converter is crucial when using TTM.

4. Structural Integration Technology

Structurally integrated motor drives have already been attempted in several fields, with significant advancements in recent years, particularly in electric vehicles, where there have been many advancements in integrated motor drives using SiC power semiconductors. However, rather than complete structural integration, developments have evolved into forms where a separate drive structure is coupled next to the motor. This chapter will address the packaging design of structurally advanced power switches that can be more directly integrated into the housing of the motor or its wires.

To achieve structural integration, basic power packaging technologies are first examined. A brief overview of the physical composition of a typical power module is provided, followed by a detailed thermal analysis of power switches to understand their thermal management requirements. The impact of parasitic components in packaging is also discussed. Building on this foundation, an Insulated Metal Substrate (IMS) based switch is designed, which reduces the mechanical layers of insulation, offering advantages in cost and weight. However, high-temperature operation is still limited by the constraints of bond wires used for interconnections. To address this issue, the application of Power Overlay (POL) technology is explored, and a new switch design suitable for integrated motor drivers is proposed. The thermal and electromagnetic designs are carried out using computer-aided design (CAD) tools.

This research is also based on the consideration of the bidirectional power switch configuration required for advanced, high-efficiency current source inverters (CSIs).

4.1 Structural Integration Design

For physical integration, lightweight power module packaging suitable for high-temperature operation is essential. Conventional multi-chip power modules use ceramics for insulation and typically consist of seven to nine physical layers. Differences in coefficients of thermal expansion (CTE) between materials can lead to cracks or lift-offs due to rapid temperature changes, reducing lifespan. While WBG power semiconductors are advantageous for high-temperature use, improved packaging design technology is needed to accommodate higher temperature variations.

Conventional Si-based power modules typically operate up to 150 degrees Celsius, with design stability usually maintained within 135 degrees Celsius. For structurally integrated motor drives aiming for a maximum operating temperature within 135 degrees Celsius, a power switch design capable of operation up to 200 degrees Celsius at the junction temperature is necessary. This study aims to design a power module suitable for high-temperature operation.

4.1.1 Power devices packaging

Power semiconductors generate significant heat during operation, which can degrade performance and shorten the lifespan of the power module package. Managing mechanical property changes, such as adhesion reduction or crack formation due to CTE mismatches between package materials, is crucial. These mismatches can cause internal crack initiation and propagation, leading to fractures, and result in warpage due to CTE differences during heating and cooling. Therefore, it is important to first examine the typical mechanical structure of a power module, as seen in Figure 4.1.

The MOSFET, featuring a vertical structure, has a source pad located at the top and a drain pad at the bottom. Consequently, a bond wire is required to connect the source pad in configurations that necessitate interconnection with other semiconductors, such as in a half-bridge or bidirectional switch. Additionally, a ceramic substrate with a lead frame is

essential for the connection and electrical insulation of the drain pad. The upper surface of the chip is finished with aluminum (Al) to facilitate Al wire bonding, while the lower surface is finished with silver (Ag) or tin-lead (Sn-Pb) for the die attach process using soldering or sintering.

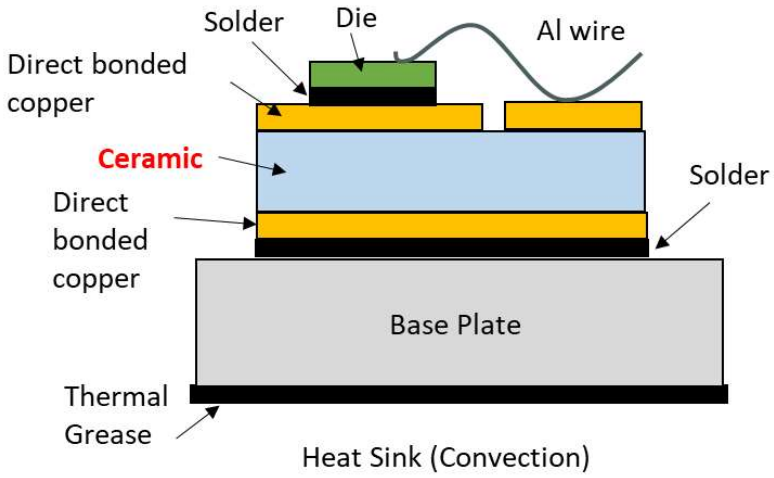


Figure 4. 1. Basic structure cross section of a power module with baseplate.

The substrate electrically connects the power device and dissipates heat generated from the power device. Bonding ceramics and copper are typically manufactured using eutectic bonding or active metal brazing (AMB) methods. Substrates are classified into Direct Bond Copper (DBC) and Direct Bond Aluminum (DBA) based on the type of metal used. Ceramic materials such as alumina (Al_2O_3) are used between the double-sided metal layers for their excellent thermal performance and insulation properties. Aluminum nitride (AlN) and silicon nitride (Si_3N_4) are also used in specific applications where matching the Coefficient of Thermal Expansion (CTE) is critical.

In a typical power module, interconnection materials are necessary for electrical connections between power devices, substrates, and power terminals. Methods such as aluminum (Al) and copper (Cu) wire or ribbon bonding are primarily used due to their excellent electrical and thermal conductivity. Heavy wires with diameters of about 300 to 500 micrometers are employed to carry higher currents effectively.

Materials like copper (Cu) and aluminum silicon carbide (AlSiC) are used to transfer the heat generated by power devices to the outside. Cooling methods include natural cooling (heatsink) or forced cooling such as fans and liquid cooling.

Table 4. 1. Characteristics of the ceramics [72]

Material	*CTE (ppm/K)*	*Thermal Conductivity* (W/mK)	*Dielectric strength (kV/mm)*	*Relative permittivity* (ε_r)	*Bending strength (MPa)*
SiC	*4.3*	*260*	*2700*	*9.7*	*500*
Al_2O_3	*6.8*	*24*	*15*	*9.8*	*350*
AlN	*4.7*	*180*	*20*	*9.0*	*360*
Si_3N_4	*3.4*	*70*	*14*	*9.2*	*700*

4.1.2 Thermal management of Power devices

In power electronic systems, temperature significantly affects the characteristics of power semiconductors, making it a crucial parameter. Exceeding the maximum junction temperature can cause damage and permanent failure, even without avalanche or short-circuit conditions. Thus, the maximum allowable junction temperature must not be exceeded.

Second, temperature also impacts conduction losses in semiconductors. For instance, the ON resistance of MOSFETs can more than double with temperature increases, leading to higher conduction losses. Additionally, the threshold voltage of MOSFETs decreases with rising temperatures, reducing control signal noise margins.

Third, repetitive operations within safe temperature ranges can induce mechanical stress, affecting solder and bond connections, and reducing component lifespan. The aging of these components is highly correlated with the extent of temperature variations.

Finally, operating temperature conditions must be considered when designing power switches, as they vary depending on the application. For example, air conditioner motors require higher currents and operate at higher temperatures in summer, while in winter,

high-frequency rotation is needed at lower ambient temperatures. In electric vehicles, frequent load variations cause rapid temperature changes in power switches, necessitating high reliability in power module design. These variations affect semiconductor losses, performance, and reliability, as shown in Figure 4.2.

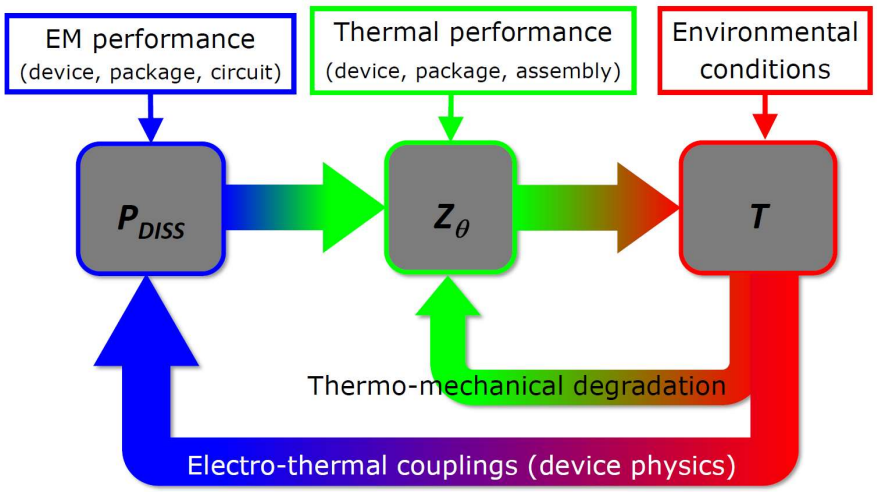


Figure 4. 2. Physical cross coupling in a power module.

Our research aims to develop power switches integrated with motor wires, requiring very high operating temperatures (125~135°C). Thus, understanding how heat generated in power semiconductors affects packaging is essential.

A. Heat generation

Heat generation in semiconductor devices involves complex mechanisms, making accurate predictions of total losses challenging. These losses include variations in conduction losses from thermal coupling and switching losses from interconnect structures. To focus the purpose of this study, the primary factor for heat generation can be expressed as Joule's heat,

$$H(\vec{x},t) \equiv \frac{P_D}{V} = \vec{J}\cdot\vec{E}\,. \tag{4.1}$$

In (4.1), P_D indicates the time and position-dependent power dissipation, V is the considered volume, $\vec{J}$ is the current density, and $\vec{E}$ is the electric field [73-74].

B. Compact thermal models

Heat propagation in semiconductor devices occurs primarily through heat conduction, convection, and radiation, with conduction being the main mode in solids due to temperature gradients. Convection involves heat transfer by the motion of a fluid, either naturally or forced, while radiation involves electromagnetic waves emitted by bodies above absolute zero.

The heat is typically generated within a subvolume of the semiconductor chip, and then, spreads across the silicon carbide die according to

$$\rho c_s \dot{T}(\vec{x},t) = \nabla\left[\lambda_{TH}\,\vec{\nabla}T(\vec{x},t)\right] + H(\vec{x},t) \tag{4.2}$$

where T is the temperature, c_s is the specific heat capacity, ρ is material density, and λ_{TH} is thermal conductivity [73-74]. While this is inherently a three-dimensional problem, it can be effectively reduced to a one-dimensional problem where heat primarily flows in the vertical direction with an approximate 45º spread angle [73-74]. This approach assumes a linear one-dimensional problem. The temperature variation ($\Delta T_j(t)$) is interpreted as the response of a linear system to the input power (i.e. the power dissipation, P_D) [75].

$$h(t) = \frac{\Delta T_j(t)}{P_D(t)} = Z_{th}(t) \tag{4.3}$$

$$T_j(t) = T_0 + \int_0^t P_D(\tau)\frac{dZ_{th}(t-\tau)}{d\tau}\,d\tau \tag{4.4}$$

where T_0 indicates the starting temperature value and $Z_{th}(t)$ the junction-to-ambient thermal impedance of the transistor. This transient thermal impedance corresponds to the system's step response and contains the full thermal system description. A power transistor's heat dissipation path from the chip to the lead frame or heat sink can be accurately represented using a transmission line equivalent circuit diagram.

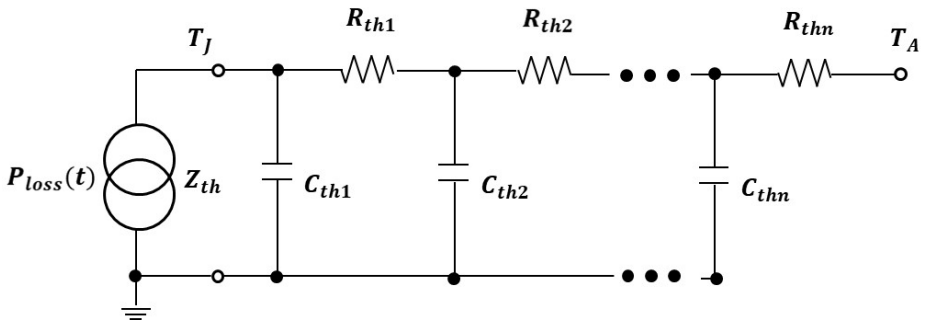


Figure 4. 3. Electrical transmission line equivalent circuit design models heat conduction properties using thermal equivalents for physical variables [75].

Therefore, the heat conduction processes can be modeled using a transmission line equivalent circuit diagram, which consists of only R/C elements, as shown in Figure 4.3. In addition, Table 4.2 shows the correspondence between electrical and thermal variables.

Table 4. 2. Corresponding physical variables [75]

Thermal		**Electrical**	
Temperature	$T\ in\ K$	Voltage	$U\ in\ V$
Heat flow	$P\ in\ W$	Current	$I\ in\ A$
Thermal resistance	$R_{th}\ in\ K/W$	Resistance	$R\ in\ V/A$
Thermal capacitance	$C_{th}\ in\ Ws/K$	Capacitance	$C\ in\ As/V$

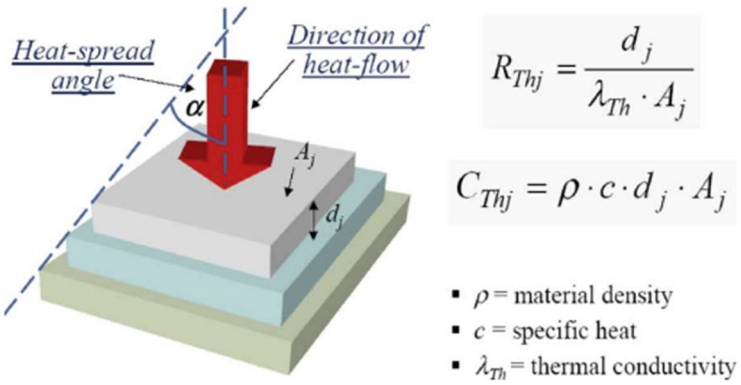


Figure 4. 4. Physical approach used for extracting the thermal impedance at chip-level. [73].

Power modules consist of multiple mechanical layers, each associated with thermal resistance (R_{th}) and thermal capacitance (C_{th}). The thickness of these layers (d_j) is selected to correspond to various physical regions identifiable within the device. When modeling thermal effects with an approximated quasi-1-D heat flow description, the lateral dimensions of each layer are derived from a given surface-active area (A_j), assuming a 45° angle for the heat wave spreading [73-75].

In bidirectional power switches, multiple devices on a common baseplate affect each other's temperature. Thermal interaction can be represented in matrix form, relating the temperature at any point to the power dissipated by all sources.

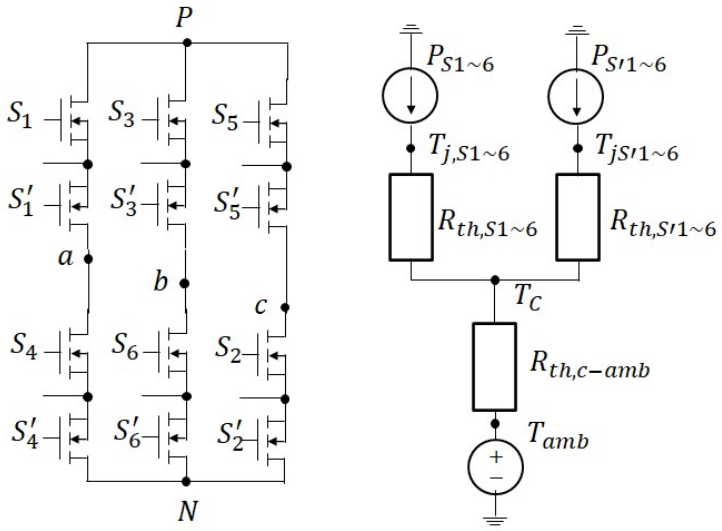


Figure 4. 5. Discrete Bidirectional electro-thermal models in CSI with bi-directional switches.

C. Heat spreader and convection

Solid heat spreaders expand the heat flow area, reducing overall thermal resistance and enhancing heat dissipation efficiency. Examples include power module baseplates and heatsinks, which amplify the heat transfer coefficient by increasing the surface area for heat exchange. This improves the thermal management, performance, and reliability of power modules.

The performance of a heat spreader depends on the size of the heat source, the material's thermal conductivity, and the heat transfer coefficient. Optimizing these factors maximizes the efficiency of the heat spreader, leading to better thermal management and system performance.

Achieving the structurally integrated design necessitates the robust cooling system with the high heat transfer coefficient. This study focuses on applications using refrigerant gas compressors or forced convection with powerful propellers for cooling.

4.1.3 Discrete Power Module Design of bi-directional Switch

A well-known challenge in developing CSI lies in employing bidirectional switches capable of bi-directional current conduction and reverse voltage blocking. Designing multi-chip power modules with such switches requires careful switching patterns and low parasitic inductance values (Figure 4.6). This challenge is amplified with the transition from Si IGBTs to fast-switching WBG semiconductors like SiC MOSFETs and GaN HEMTs.

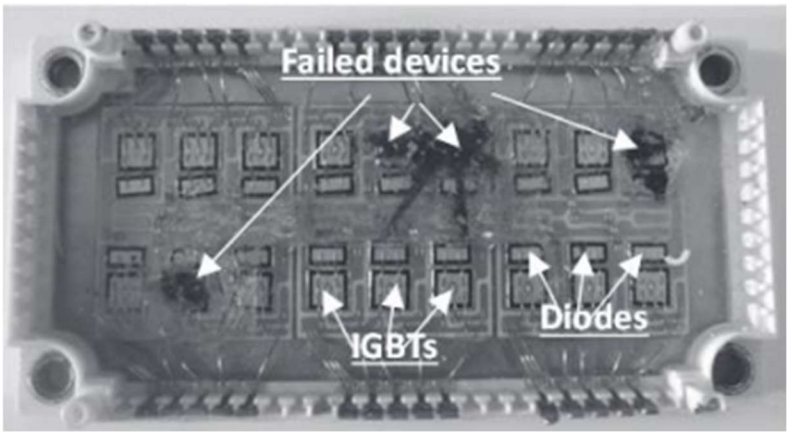
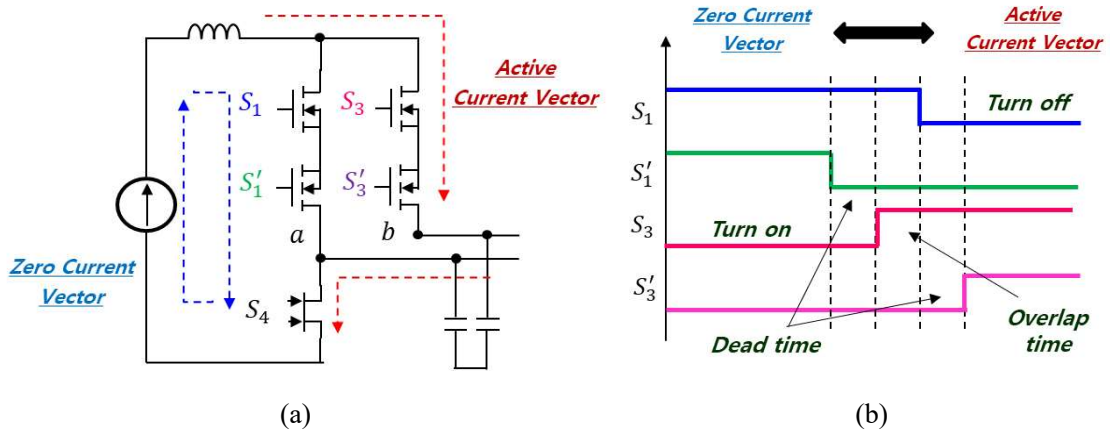


Figure 4. 6. Multi-phase Si-IGBT plus Si-Diode BDS power module failed as a result of loop parasitic inductance and faulty switching sequence [76].

Unlike HBS (Half-Bridge Switch), Deploying BDS requires evolved switching sequences to avoid short-circuit or open-circuit events, crucial for containing parasitic

inductance in current commutation paths. Specific care is needed to avoid failures such as short-circuit/shoot-through or open circuit effects, which can cause destructive overcurrent or overvoltage conditions. A four-step commutation sequence ensures proper dead-times and overlap times between switches, as shown in Figure 4.7 [76,77].



(a) (b)

Figure 4. 7. (a) Circuit diagram of current commutation between two phases of a CSI: the blue dashed line indicates the current flow before the commutation and the red dashed line the current flow path after commutation; (b) corresponding switching sequence and CSI vector states.

In Figure 4.7 (a), assuming S_4 is always on during the transition and the load current initially flows over $S_1 - S_1'$ and S_4, with the direction indicated by the blue arrows. When $S_1 - S_1'$ must be turned off and $S_3 - S_3'$ turned on, as displayed by the red arrows. As indicated in Figure 4.7 (b), the correct switching sequence must be:

1) Turn off S_1' while maintaining current flow through the body-diode of S_1'.

2) Turn on S_3 to prepare an alternative current flow path over S_3 and the body-diode of S_3'.

3) Turn off S_1 and diverting the current to $S_3 - S_3'$.

4) Turn on S_3' to achieve the lowest on-state voltage drops.

The presence of stray inductance components in the current commutation loop interferes with the actual device turn-on and turn-off times, as well as with the time it takes for the current to actually divert from $S_1 - S_1'$ to $S_3 - S_3'$. This is a critical point, typically

leading to switching failures in these architectures. Therefore, to achieve high-speed switching, a low-impedance design for the interconnections must be considered, as shown in Figure 4.8. In this work, a higher level of modularity is pursued, and the integration effort is initially focused on the single BDS.

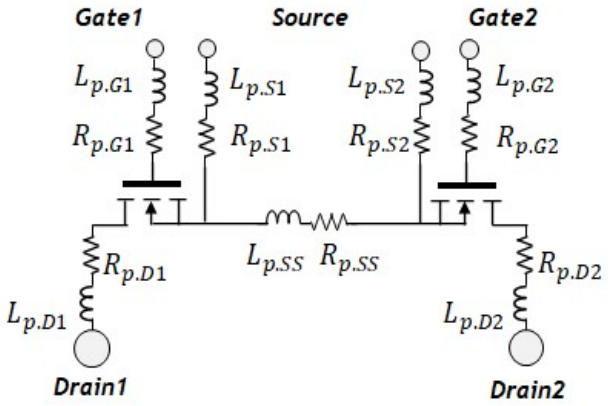


Figure 4. 8. The lumped circuit model of the advanced current source inverter with the Bidirectional Power Switch (BDS).

4.2 Insulated Metal Substrate (IMS) based lightweight power module

This section presents the design and development of a Bidirectional Switch (BDS) using Insulated Metal Substrate (IMS) technology. The switch features an aluminum (Al) baseplate with an insulation layer, which is a cost-effective alternative to ceramic substrates such as direct bonded copper (DBC). This approach not only provides a competitive edge in terms of cost but also offsets the higher expense of Wide Bandgap (WBG) semiconductor technology compared to silicon (Si) through savings at the packaging level.

4.2.1 IMS-based power module design

A power module includes a substrate with semiconductor dies attached, providing electrical terminations, efficient heat transfer, and insulation from coolant. Direct bonded copper (DBC) substrates, common in high-power applications, are prone to cracking from mechanical and thermal stress and have higher thermal resistance due to their thickness.

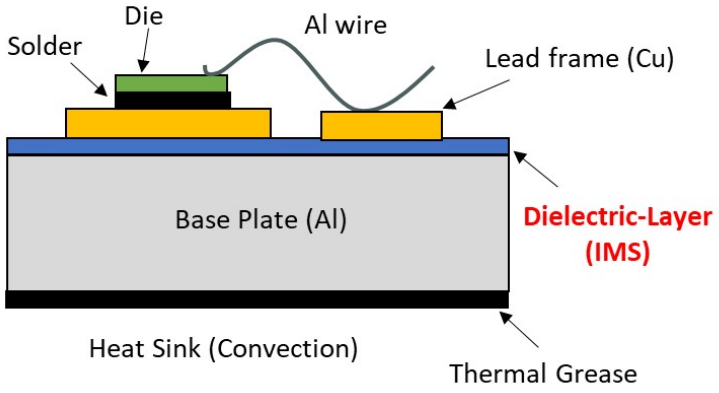


Figure 4. 9. Vertical cross-section view of Insulated Metal Substrate (IMS) based power module

An insulated metal substrate (IMS)-based power module uses a polymer-based thin insulating material, offering reduced mechanical layers with increased flexibility, as shown in Figure 4.9 [78]. Compared to ceramic insulators, polymer insulators have a higher

breakdown voltage and can be manufactured in thin layers, making IMS a cost-effective solution for wide-band-gap (WBG) high-power applications.

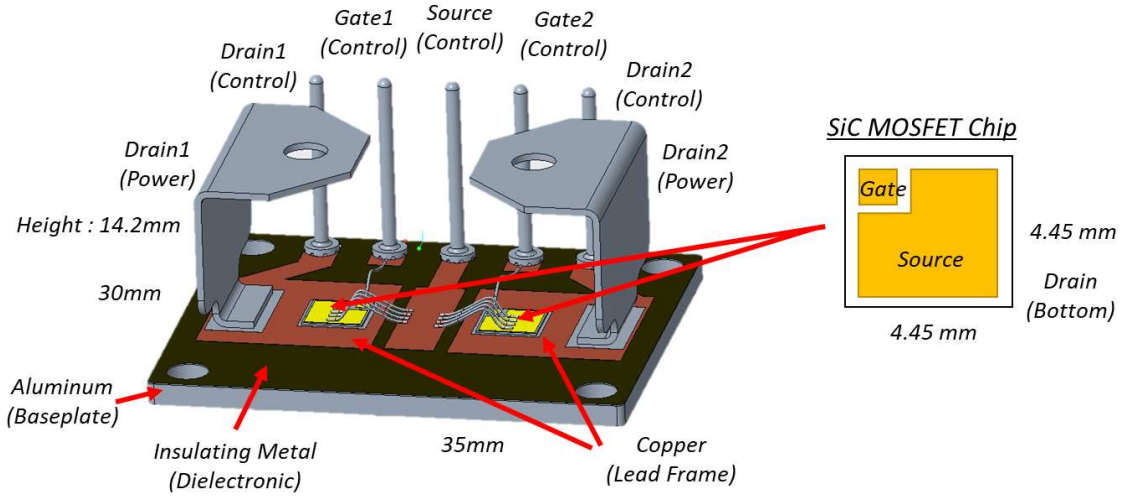


Figure 4. 10. IMS-based bi-directional power module design

In designing a 15 kW-rated buck-CSI for a modular integrated motor drive with a switching frequency of $f_s = 75\,kHz$, $750V - 15m\Omega$ SiC MOSFETs were used (Figure 4.10). Custom-designed bidirectional SiC power modules require low inductance and interconnection resistance for fast switching. Power terminals are designed for low-parasitic inductance bus-bar interconnection and 3D system-level assembly. In the prototype, power terminals are soldered onto the IMS with pins for driving and sensing.

Unlike DBC, IMS-based power modules eliminate a ceramic layer, reducing weight and production costs. However, the poor thermal conductivity of insulating metal layers requires careful electro-thermal and electromagnetic analysis during design.

4.2.2 Electro-Thermal design

The primary thermal response considered in this study is the junction temperature of the power semiconductor, with heat generation assumed to originate primarily from the

upper part of the device. Therefore, the top surface of the two source pads was designated as the heat generation region. A heat sink attached to the lower surface of the bottom aluminum layer provides additional heat dissipation, and the module's boundary condition was specified based on convection.

Power modules with multiple heat sources may experience mutual heat interference depending on dissipation conditions, making it essential to monitor temperature variations using 3D CAD. The key physical properties of the constituent material layers are summarized in Table 4.3 [67-68].

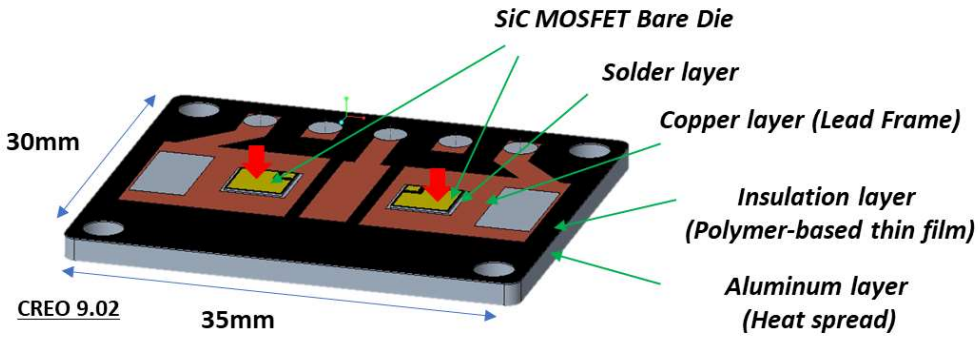


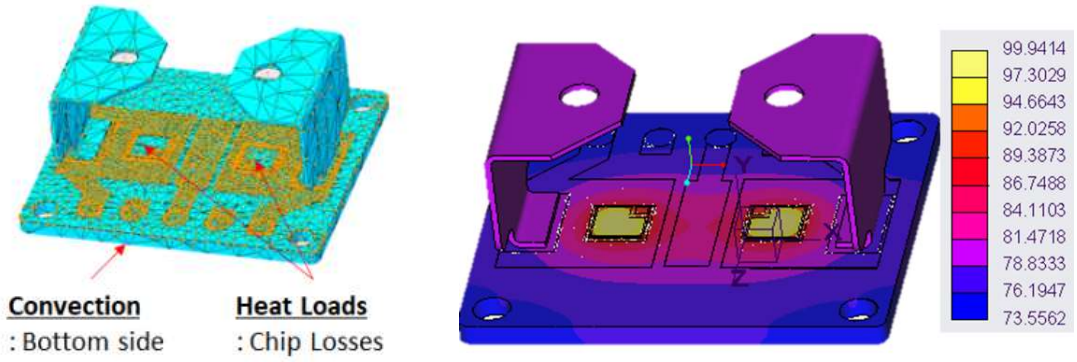
Figure 4. 11. Insulated Metal Substrate based bi-directional power module design

Table 4. 3. Representative properties of the various materials used in the bi-directional switch assembly

	Material	*Density [ρ, kg/m3]*	*Specific Heat Capacity. [cs, J/kg K]*	*Thermal Conductivity [λ, W/m K]*	*Thickness [mm]*
1	*SiC*	*3,211*	*690*	*370*	*0.18*
2	*Solder (Sn-Pb)*	*7,500*	*220*	*59*	*0.075*
3	*Cu*	*8,930*	*385*	*388*	*0.035*
4	*Insulating Material*	*1,024*	*1,624*	*10*	*0.1*
5	*Al*	*2,707*	*905*	*200*	*1.55*

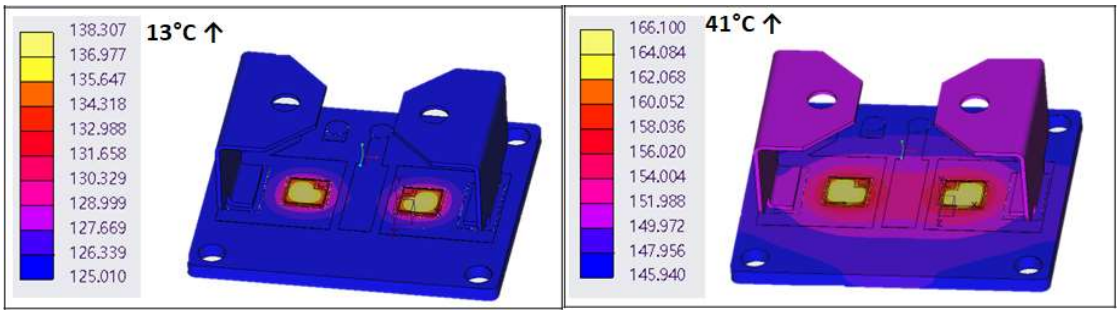
Consequently, it is crucial to monitor the temperature variation of the designed module using 3D CAD. As depicted in Figure 4.12 (b), the conditions leading to semiconductor

temperature changes of 100 degrees under natural convection coefficient ($h = 400W/m^2K$) were observed at power losses of a total of 64W (each with a loss of 32W). These thermal simulations were performed based on the CREO software [79]. The obtained simulation result shows that thermal resistance can be explained by 1.563 K/W under natural convection conditions.



(a) (b)

Figure 4. 12. (a) A mesh plot of IMS-based BDS for the thermal analysis (b) Simulated surface ΔT evolution in the case of heat load each 32W and convection coefficient $h = 400W/m^2K$.



(a) (b)

Figure 4. 13. (a) The simulation shows the results of thermal analysis under optimal convection conditions (i.e., $h = 50kW/m^2K$) in the case of heat load each 25W with 125°C initial boundary condition. (b) the results depict the outcomes with a relatively low convection coefficient ($h = 1kW/m^2K$) at the same condition in the heat load, revealing interference between each chip.

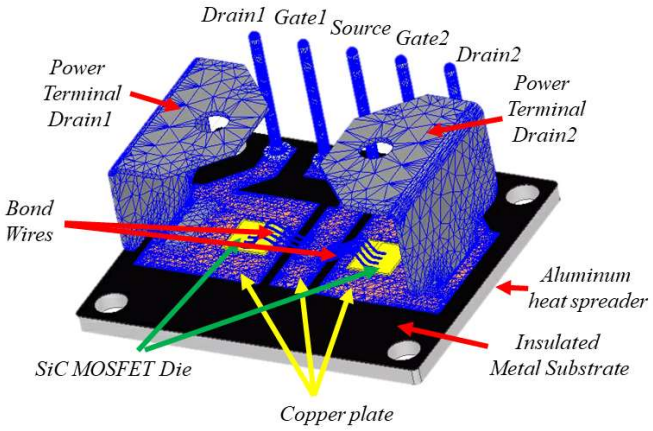
For the purpose of structural integration design in this study, simulations were conducted to ensure that the maximum temperature of MOSFETs in power modules with bond wire and solder layers, operating under 125°C boundary conditions applicable to compressors, does not exceed 175°C. Considering the maximum power of 15 kW for the compressor motor and assuming an efficiency of 98% based on previous research [53] on 3-phase BDS-based CSI, the total losses are estimated at 300 W with 6 BDSs, resulting in a load per BDS of up to 50 W. Therefore, assuming 25 W of heat load per chip, simulations under worst-case conditions were performed as shown in thermal analysis simulation Figure 3.18, considering two heat transfer coefficients. Even under conditions that might not be optimal, as shown in Figure 4.13(b), the maximum temperature remains within 166°C, which is an increase of 41°C, predicting operation within 175°C limits.

4.2.3 Electro-Magnetic design

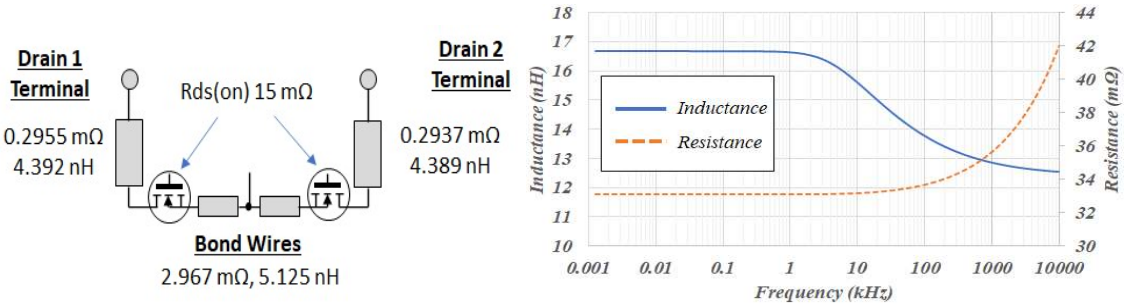
The module necessitates a connection between the source pads of the two MOSFETs, along with a connection pin facilitating the control of each switch's gate. Typically, bond wires are employed for this purpose, but they can inadvertently introduce parasitic components. Moreover, if the interconnection resistance is substantial, it may give rise to operational issues. Therefore, the designed module uses a copper plate to connect each source pad with standard bond wires to mitigate interconnection parasitic components. Further, due to the vertical structure of the SiC MOSFET, the Drain is situated on the bottom surface of the chip. To mitigate interconnection resistance and enhance design efficiency, a copper plate is utilized to link the Drain to the power terminal. This assembly is then positioned atop the Insulated Metal Substrate (IMS), as you can see in Figure 4.14(a).

In this investigation, we employed the Ansys Q3D Extractor software tool [80], utilizing finite element analysis (FEA) techniques, to assess the interconnection resistance and parasitic inductance within this design. To assess the interconnection resistance and inductance along the current conduction path, the top surface of power terminal drain 1 in Figure 4.14(a) is designated as the source. This surface is linked to the SiC MOSFET Die through an aluminum bus bar and a copper plate, while the bottom surface is assigned as

the sink. Furthermore, as the conduction current flows through interconnected bond wires using a common source copper plate, the lower surfaces of the bond wires in contact with the left SiC MOSFET source pad are declared as sources, and the lower surfaces of the bond wires in contact with the opposite SiC MOSFET Die are designated as sinks.



(a)



(b) (c)

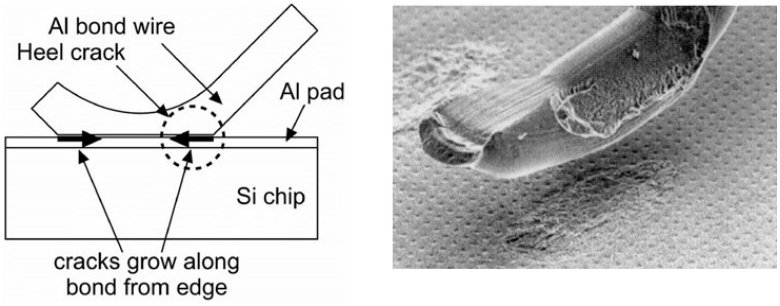
Figure 4. 14. (a) Ansys Q3D Extractor ACL/R mesh plot of the designed SiC-MOS BDS: the transistors are soldered drain side onto the IMS and bond-wires (ultrasonic bonding) are used for the source and gate interconnections, (b) Results of inductance and resistance simulation for each major interconnect part analyzed at 75 kHz, (c) Results of inductance and resistance simulation over frequency.

In the final configuration, the lower surface of the right SiC MOSFET Die is set as the current source, and the upper end of power terminal drain 2 is identified as the sink. This arrangement facilitates the extraction of parasitic components for each interconnection when current is conducted from drain 1 to drain 2. Every conduction path is identified and

assigned a unique number as "i". Based on the simulation results, it has been possible to analyze the interconnection components in the i-by-i matrices at 75kHz, which is a potential switching frequency, and the summarized result can be seen in Figure 4.14(b). Ultimately, as all current conduction paths are interconnected in series, the cumulative resistance and inductance can be determined by summing up over the frequency the extracted mutual resistance and inductance, as in Figure 4.14(c). It's assumed to note that the on-resistance of the power semiconductor is presumed to be a constant 15 mΩ, and it remains unchanged over the frequency. Based on the simulation results, assuming a switching frequency of 75 kHz and an on-resistance of 15mΩ for the power semiconductors, the total parasitic interconnection resistance is predicted to be approximately 34mΩ. Additionally, the parasitic inductance is estimated to be around 14nH.

4.3 Power Overlay based high-temperature power module design

However, even with IMS, soldering and bond wires remain unavoidable in multi-chip designs. Consequently, despite the high-temperature operation capability of WBG power semiconductors, if soldering and bond wires are still used as in conventional power module packaging, the maximum permissible temperature will be the same as that of traditional Si-based power modules (typically within the range of 150°C to 175°C). For example, when bond wires are used, the repeated temperature changes in power semiconductors cause the bond wires to develop cracks starting from the edges and eventually lift off at the ends, as shown in Figure 4.15. This phenomenon can occur more rapidly if wide-band-gap (WBG) power semiconductors are operated at even higher temperatures. Additionally, bond wires are a significant source of parasitic elements. Therefore, this study investigated the structural integration using Power Overlay (POL) technology, which enables higher temperature operation.



(a) (b)

Figure 4. 15. (a) Crack propagation direction in Al-bond wire lift-off and (b) Scanning electron microscope (SEM) image of bond wire lift-off [81,82]

4.3.1 Power Overlay Technology

Power Overlay (POL) is a specialized packaging technique for power semiconductors that uses printed circuit board (PCB) manufacturing technology for electrode connections and wiring, as shown in Figure 3.27. POL enhances low conduction resistance and high-

speed switching performance for power semiconductors, including traditional silicon (Si) devices and newer materials like silicon carbide (SiC) and gallium nitride (GaN). This technology facilitates the development of power supply units with low conduction loss, low switching loss, short switching dead time, and high heat dissipation, enabling compact, lightweight, highly efficient power systems with long operational lifetimes. These strengths are particularly well suited for high-speed switching and high-temperature operation of WBG devices.

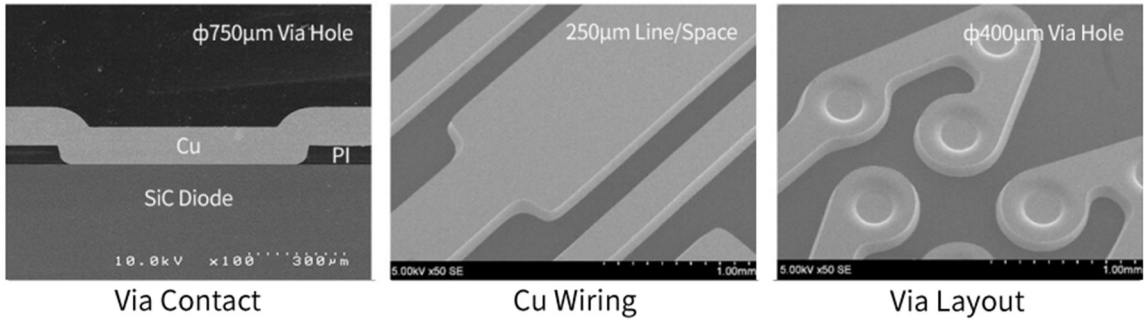


Figure 4. 16. The three key features of POL technology are (a) Via Contact: Connections to power devices, (b) Cu Wiring: Copper patterns similar to those used in PCBs, (c) Via Layout: Configuration examples for connecting passive components or power devices [83].

Here, key features of POL include:

- High-Temperature Capability: Suitable for extreme conditions required by WBG devices.
- Low Parasitic Inductance Interconnects: Essential for high-speed switching applications.
- High Switching-Frequency Capability: Allows efficient operation at high frequencies.
- Multi-layer Current Sharing Capability: Reduces parasitic capacitance, improving overall performance.
- Micro-meter Scale Interconnect Capability: Critical for devices such as GaN HEMTs.
- Embedding of Decoupling Capacitors and Gate Drivers: Ensures electromagnetically clean and low-loss switching transitions.

The POL process enables the creation of extremely small features with high precision and reproducibility. Figure 4.17 shows an example of these features in a sample assembly. The flexible interlayer substrate, made from Kapton polyimide film, contains vias formed

by laser ablation and then metalized through sputtering or plating to establish interconnections. This method does not require specific preparation or alteration of the top metal layer of the power devices. Surface-mount devices (SMDs) can be placed directly on top of the power devices or at highly controllable distances, minimizing stray inductance.

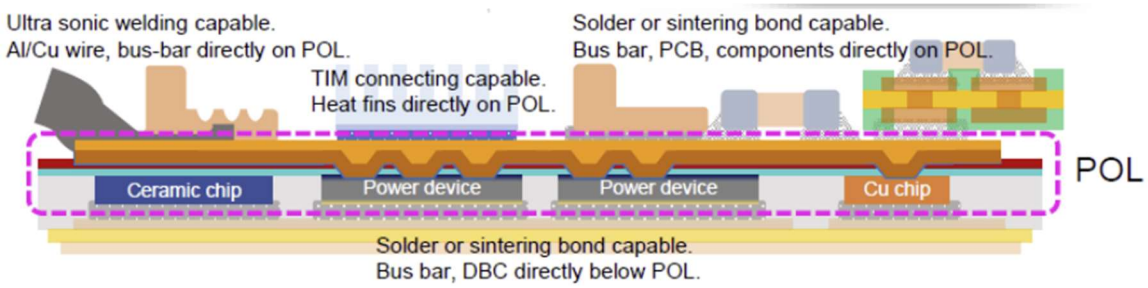


Figure 4. 17. Illustration of the concept of Power Overlay Technology (POL) [83].

4.3.2 POL-based BDS design for the structural integration

The main objective of this study is to implement a structurally integrated design of motor wires and power switches. Previous research using POL technology has primarily focused on combining power devices with DBC for insulation and heat transfer, as like Figure 4.18.

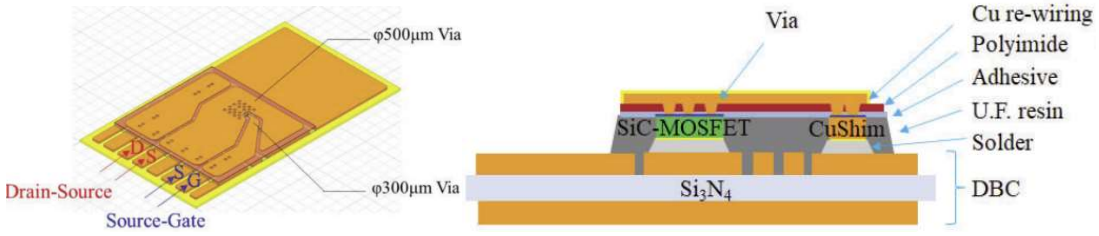


Figure 4. 18. Structure image and cross-section schematic view of POL [84].

Although previous studies have significantly increased power density using POL technology, they ultimately required the use of DBC for cooling system integration and lead frame insulation.

This study's main idea is to directly combine motor wires with power semiconductors without using DBC, as shown in Figure 4.19. Motor wires are primarily made of copper, which has a thermal conductivity similar to that of SiC, enabling rapid heat transfer. If the motor's heat transfer coefficient is sufficiently high, directly coupling motor wires with drastically reduced mechanical layers can significantly lower thermal.

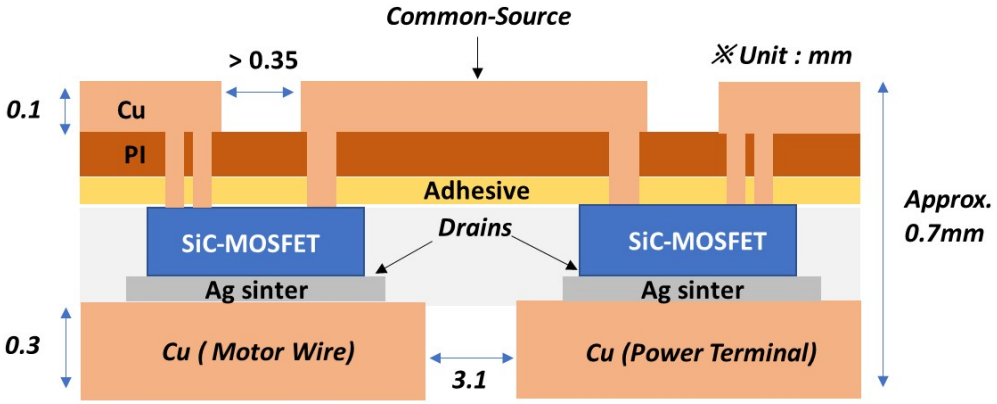
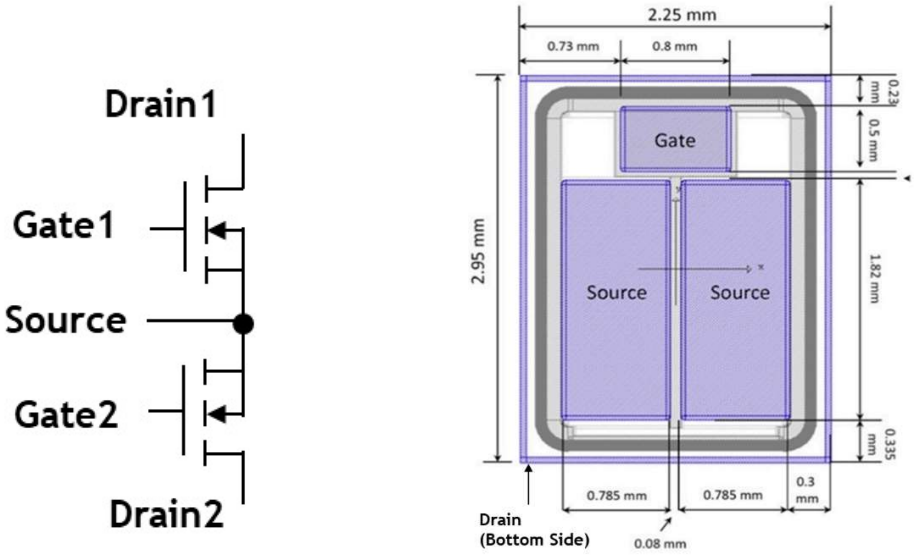


Figure 4. 19. Illustration of the cross-section view of designed Power Overlay (POL) based bi-directional switches.

Considering the direct connection with the motor, this study designed a discrete BDS to allow for more flexible connections. The circuit of the BDS features a common source and drain power terminals on both sides, as shown in Figure 4.20 (a). The devices used in this work are Wolfspeed CPM3–0900-0065A in bare-die from [85], with nominal $V_{DS} = 900\ V$ and continuous drain current $I_D = 23\ A$ at 100 °C. The chip structural features are shown in Figure 4.20 (b).

The BDS design, as depicted in Figure 4.19, presents a unique cross-sectional view. This view not only reveals the various constitutive materials and layers but also showcases an innovative top-side interconnection strategy for the gate and source terminals. A notable feature is the introduction of two separate interconnection points for the source terminal, one for the gate driver and one for the power source terminal. This design is a significant departure from conventional designs as it effectively prevents any influence of the load current di/dt on the gate-drive loop during switching. The concept is akin to the Kelvin-

source connection used in the latest discrete commercial packages for SiC power MOSFETs (4-pins TO-247 [86]), a design choice that has been universally adopted by all the major manufacturers. Furthermore, the drive source terminal is divided into two symmetrical parts to align with the device's structural features (Figure 4.20 (b)), ensuring a more uniform turn-on and off of all the cells in the chip.



(a) (b)

Figure 4. 20. In (a), schematic of MOSFET BDS in common source configuration, in (b), image of SiC MOSFET chip with indication of lateral dimensions (units is mm) [85].

On the bottom side, the SiC dies are sintered onto flat copper (Cu) bars, corresponding to the BDS power drain terminals.

The copper bars are designed to simulate the flat structure of motor wires. However, not all motors use flat wires; many motors use round wires, which necessitates mechanical ingenuity for proper connection. For instance, designing additional structures on the cross-sectional copper bars is conceivable to enable coupling with round motor wires. This study focused on the power switch design and used copper bars for the analysis.

The integration with motor wires employed Ag sintering technology, a method more suitable for use at higher temperatures than traditional soldering. Ag (Silver) sintering, a technique used to join electronic components and power semiconductors, is a prime

example of the superior properties of silver. This process involves sintering silver nanoparticles or microparticles under high temperature and pressure to form a robust metallic bond. The stability of silver sintering at high temperatures makes it ideal for power semiconductors that operate in high-temperature environments. The superior electrical and thermal conductivity of silver further enhances the performance of electronic components, a fact that we should all appreciate in our field.

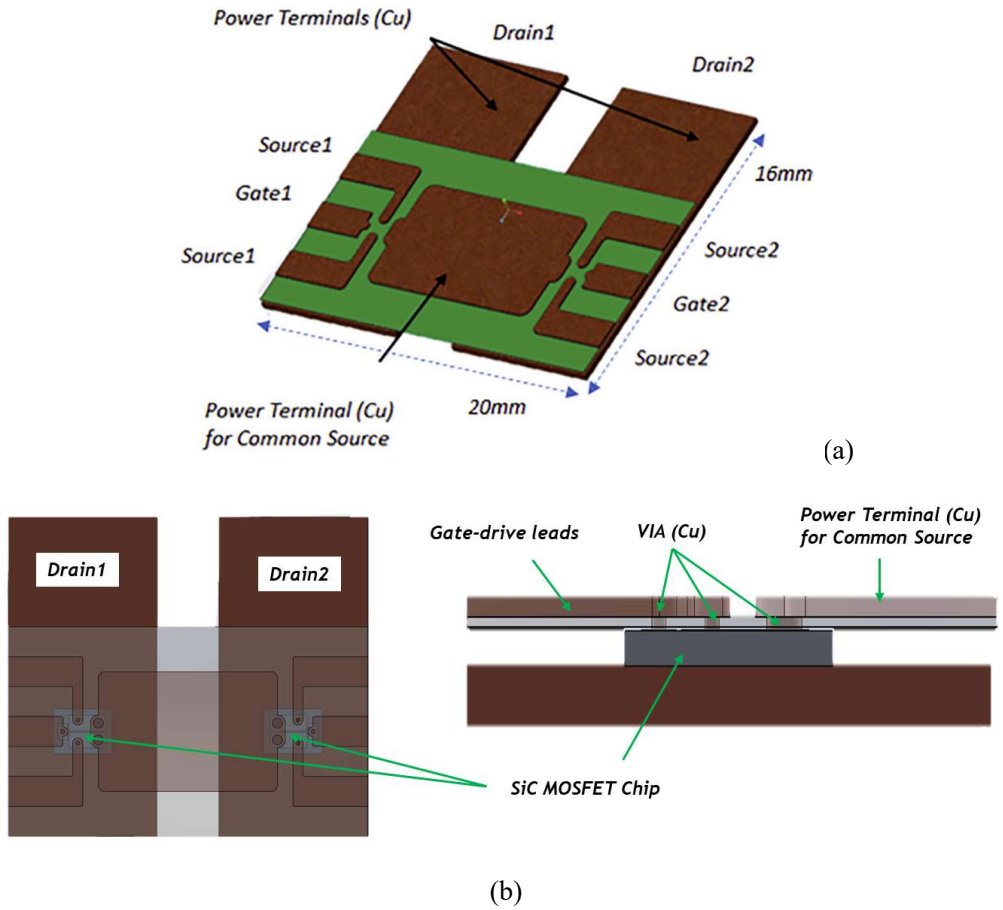


Figure 4. 21. Illustration of 3D module structure with an indication of lateral dimensions.

Unfortunately, the manufacturing company has not disclosed the precise composition of the adhesive layer located between the PI layer and the SiC device. However, it has been determined that this adhesive layer is 40 µm. Although the exact material is undisclosed, this thickness is not anticipated to impact the thermal design significantly. In Figure 4.21, a top-side view of the assembly is shown, indicating the overall lateral dimensions.

4.3.3 Electro-Thermal Simulation

In the context of incorporating the integrated design with motor wires and the power module, it is essential to consider the motor wire's thermal limitation. Therefore, for the purpose of this study, the initial boundary temperature has been established as 135 °C. Figure 4.22 shows the results of the steady-state simulation: here, the power dissipation in the chip is 10 W; the initial temperature is set at 135 °C, and the boundary conditions are emulated by a convection coefficient $h = 2\ kW/m^2K$ applied to the bottom Cu terminals (drain interconnects), whereas all other surfaces are treated as adiabatic. The results confirmed a peak temperature variation within the design intentions (i.e., 200 °C) under these conditions.

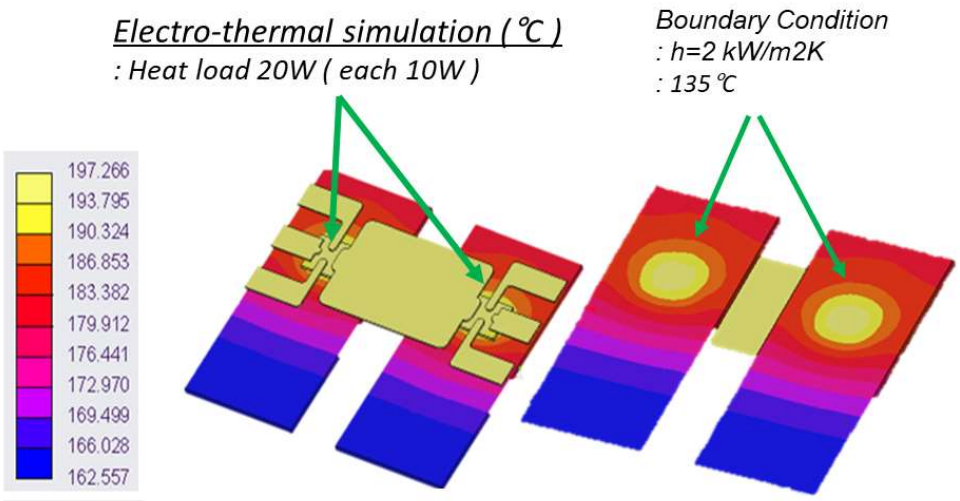


Figure 4. 22. The electro-thermal simulation. The bottom of each drain pad is exposed to convection conditions by a convection coefficient of 2 kW/m^2K. The temperature distribution is depicted in Celsius.

As mentioned in the previous section, the power module design considers systems with superior thermal conductivity, such as liquid cooling or direct attachment to the motor winding. The transient response characteristics of the junction temperature about the convection coefficient are depicted in Figure 4.22. The power module, when attached to the motor's stator, facilitates active heat dissipation through the rotation of the motor rotor.

However, future considerations should be made to incorporate additional heat dissipation designs, considering the specific structure of the motor connection. Moreover, the heat load considered in this study was based on a 3-kW rated power of the three-phase inverter with 10 W per chip.

Table 4. 4. Representative properties of the various materials used in the POL-based bi-directional switch assembly [87-90]

	Material	*CTE (ppm/K)*	*Density [ρ, kg/m3]*	*Specific Heat Capacity. [cs, J/kg K]*	*Thermal Conductivity [λ, W/m K]*	*Thickness [mm]*
1	*SiC*	*4.3*	*3,211*	*690*	*370*	*0.18*
2	*Ag (sintering)*	*18.9*	*10,490*	*236*	*175*	*0.03*
3	*Cu*	*16.5*	*8,930*	*385*	*388*	*0.3*

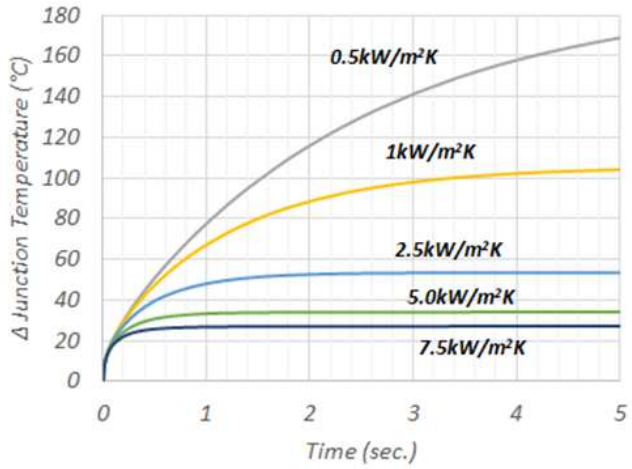


Figure 4. 23. The electro-thermal simulation demonstrates the variation in junction temperature across different convection coefficients, while main training a heat load of 10W for each chip.

Table 4.4 provides detailed information on the materials used in the simulation. As discussed earlier, the number of mechanical layers has been significantly reduced, with only four layers, including the vias (Cu), for interconnection. This is almost half the number of layers in conventional DBC-based power modules. Consequently, the thermal resistance from the MOSFET's junction to the bottom of the motor wire (case) is considerably low,

estimated at around 0.17 K/W, assuming a heat dispersion angle of approximately 45 degrees.

As a result, the temperature difference between the junction and the lower part of the motor wire referred to as the case, is minimal. Additionally, as shown in Table 3.6, the mechanical layers are fewer, and the CTE (Coefficient of Thermal Expansion) variations between materials are minor. This implies that the design is expected to exhibit a high level of robustness against repeated thermal cycling.

4.3.4 Electro-Magnetic Simulation

To facilitate rapid switching, wide-band-gap power modules face challenges in minimizing parasitic impedance. Compared to conventional silicon-based power modules, the higher switching frequencies of these wide-band-gap devices result in increased spike voltages due to stray inductance. The Power Overlay (POL) technique offers an advantage in reducing parasitic impedances by eliminating the need for bond wires in the design. In this study, we utilized Ansys Q3D Extractor to evaluate the parasitic impedances.

Through simulation, the parasitic parameters of copper metal pads, excluding the internal parameters of the power semiconductors, were analyzed. The current input area was designated as the Source, while the connected output plane was defined as the Sink. A uniform current was applied through the input source. The simulation results for each component are summarized in Figure 4.24 (b).

The parasitic parameters associated with the main power conducting path, from Drain1 to Drain2, can be estimated by combining the relevant interconnection inductance and resistance. Considering the *Rds.on* resistance of 65mΩ for each SiC MOSFET power semiconductor (at $T_j = 25°C, V_{gs} = 15V, I_d = 20A$), the total interconnection resistance of the designed module is approximately 130mΩ, with the connection resistance being less than 1mΩ. Additionally, the stray inductance is observed to have a small value of only 3.92nH (@75 kHz), as determined by the sum of the stray inductance between the Drain1

Power terminal to the Drain1 Pad, the Source1 Pad to the Source2 Pad, and the Darin2 Pad to the Drain2 Power Terminal in Figure 4.24 (b).

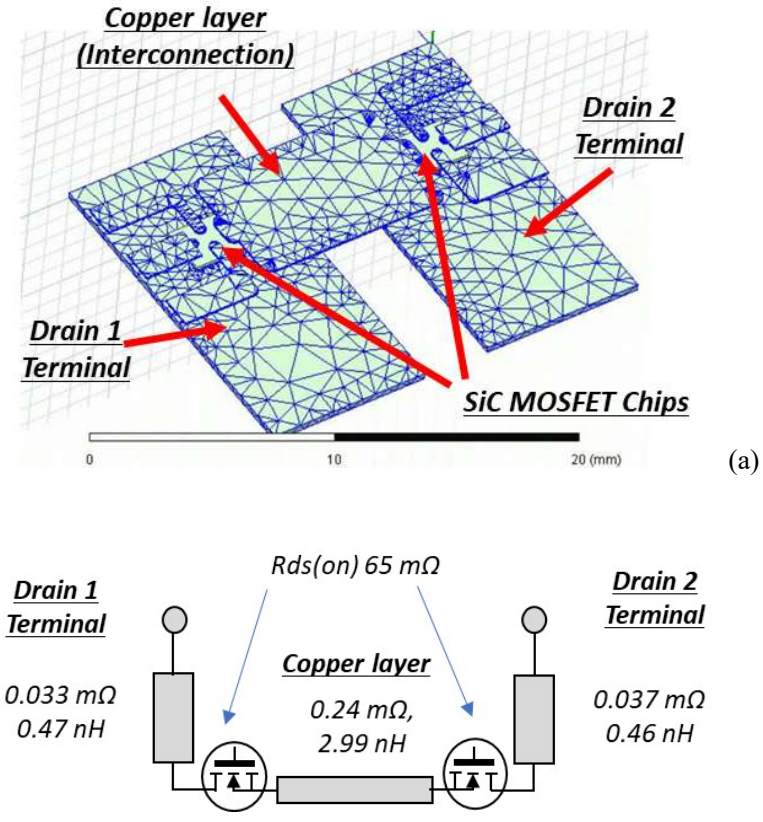


Figure 4. 24. Electro-Magnetic Simulation. In (a), the image shows the Ansys Q3D Extractor ACL/R mesh plot of the designed SiC-MOS BDS. In (b), the figure presents the inter-connection inductance and resistance, which correspond to the parasitic parameters of each connection at the switching frequency (i.e., 75 kHz).

It is important to note that the parasitic components may vary with different frequencies. In Figure 4.25, the characteristics of the interconnection inductance and resistance are presented across a range of frequencies. This includes the combined values from the Drain1 Power terminal to the Drain1 Pad, the Source1 Pad to the Source2 Pad, and the Drain2 Pad to the Drain2 Power Terminal. These combined values represent the sum of the respective parasitic components.

This study compared simulation results with data from a previous study by Y. Nishihara and other researchers to assess the parasitic inductance of POL and bonding wire in power switches, as shown in Table 4.5. The previous study [91] also reported lower parasitic inductance at the same size as wire bonding at 1 MHz. While the design in this study structurally differs from previous research, making direct size comparisons challenging, it yielded similar results. This confirms that the design in this study exhibits very low parasitic inductance compared to existing technologies.

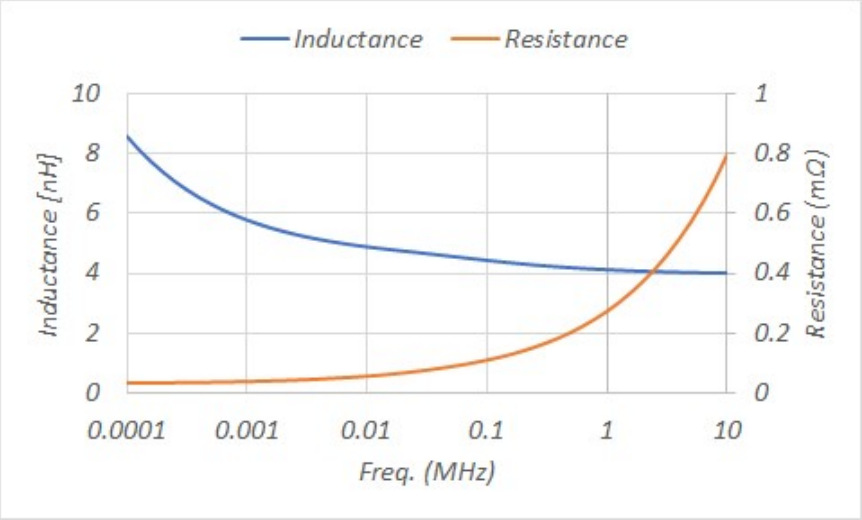


Figure 4. 25. Electro-magnetic simulation with diverse frequency.

Table 4. 5. Comparison of the parasitic inductance with previous study data [91]

	Proposed POL-based BDS design	***POL with DBC***	***Wire bonding***
Inductance (nH, @1MHz)	*4.1*	*4.71*	*10.13*

5. Functionally advanced motor modular drive system

In this chapter, we discuss the design of motor controllers using the high-speed switching capabilities of Wide Bandgap (WBG) semiconductors. The primary advantage of WBG is the ability to achieve high-speed switching, which allows digital controllers to approximate continuous time control, thereby improving control performance. First, we will review the fundamental motor control theories and explore Field-Oriented Control (FOC), which is widely used in three-phase Permanent Magnet Synchronous Motors (PMSMs).

Building on this understanding, we will examine the control differences between traditional Voltage Source Inverters (VSIs) and Current Source Inverters (CSIs). Unlike VSIs, CSIs include output filter capacitors, which introduce control differences. Typically, complex multi-loop controllers that require both voltage and current sensors are used due to these differences. We will explore these aspects in detail.

Finally, we propose a simplified controller that relies solely on capacitor voltage sensors, eliminating the need for output current sensors. This controller leverages high-speed sampling and switching, made possible by WBG semiconductors, to enhance control performance while reducing system complexity.

5.1 Vector Control of Permanent Magnet Synchronous Motor

One of the primary objectives of this study is to design an advanced motor controller utilizing the high-speed switching capabilities of wide bandgap (WBG) semiconductors. Therefore, this section will first explore general motor control theory. Although there are various types of motors, this study will focus on permanent magnet synchronous motors (PMSMs) due to their high-power density and high efficiency, making them suitable for numerous industrial and household applications.

5.1.1 Motor Control

An electric motor is a device that converts electrical energy into mechanical rotational force (torque) at the output shaft [92-93]. The torque generated by the motor (T_e) is transformed into speed (ω_{rm}) after being filtered by the mechanical system's inertia (J) and friction (B) coefficient, as shown in Figure 5.1.

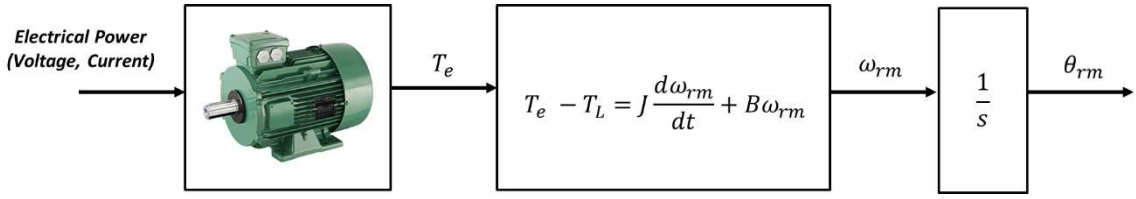


Figure 5. 1. Basic energy transfer process in a motor system: electrical power → electromagnetic conversion → torque generation → mechanical output.

A. Modeling of the DC motor

Firstly, a representative motor control system can be briefly explained using a DC motor model, as shown in Figure 5.2. The armature voltage (V_a) can be explained in Eq. (5.1), which consists of three components; The voltage drops across the armature resistance $R_a i_a$, the inductive voltage $L_a \frac{di_a}{dt}$, and the back electromotive force (EMF) e. The armature

voltage is controlled to regulate the motor speed. By adjusting V_a, we control the armature current i_a, which in turn influences the motor torque (T_e).

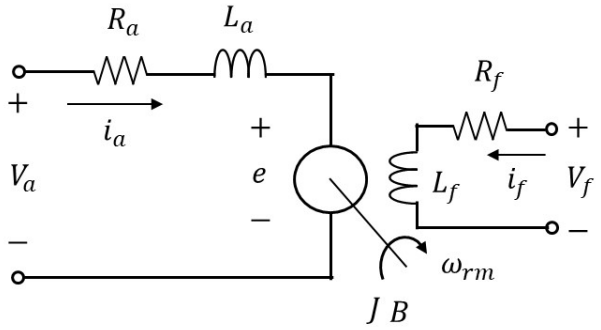


Figure 5. 2. The Steady-state model of the DC motor.

$$V_a = R_a i_a + L_a \frac{di_a}{dt} + e \tag{5.1}$$

Eq. (5.2) describes the field voltage (V_f), which includes the voltage drop across the field resistance $R_f i_f$ and the inductive voltage $L_f \frac{di_f}{dt}$. The field voltage is applied to the motor's field winding. The field winding is typically made up of many turns of wire, creating a magnetic field when current flows through it.

$$V_f = R_f i_f + \frac{d\lambda_f}{dt} = R_f i_f + L_f \frac{di_f}{dt} \tag{5.2}$$

The field current flows through the field winding and establishes the magnetic field in the motor. The strength of this magnetic field is proportional to the field current, which in turn influences the motor's operation. The magnetic flux linkage λ_f is given by:

$$\lambda_f = f(i_f) = L_f i_f \tag{5.3}$$

In many practical cases, the relationship between the field current i_f and the flux linkage λ_f is linear. This is the field current determines the strength of the magnetic field produced by the field winding. A higher field current results in a stronger magnetic field, which increases the back EMF and the torque produced by the motor.

The back EMF e is given by

$$e = k\lambda_f \omega_{rm} = K_e \omega_{rm} \tag{5.4}$$

In (5.4), k is a constant and ω_{rm} refers the rotor mechanical speed. Since $\lambda_f = L_f i_f$, the back EMF is proportional to the field current and the rotor speed. A higher field current increases the back EMF for a given speed, which in turn influences the armature voltage.

The electromagnetic torque T_e is directly related to the armature current i_a and the product of the flux linkage λ_f, which depends on i_f.

$$T_e = k\lambda_f i_a = K_T i_a \tag{5.5}$$

Eq. (5.6) shows the electrical motor of motion, where J is the moment of inertia, B is the damping coefficient, and T_L is the load torque.

$$T_e = J\frac{d\omega_{rm}}{dt} + B\omega_{rm} + T_L \tag{5.6}$$

From these equations, we derive the transfer function that relates the rotor mechanical speed to the armature voltage.

$$\frac{\omega_{rm}(s)}{V_a(s)} = \frac{K}{(sL_a + R_a)(Js + B) + K^2} \tag{5.7}$$

$$\frac{\omega_{rm}(s)}{V_a(s)} \approx \frac{K}{(sL_a + R_a)Js + K^2} = \frac{\frac{K}{JL_a}}{s^2 + \frac{R_a}{L_a}s + \frac{K^2}{JL_a}} \tag{5.8}$$

Where K is a constant related to the motor torque constant and back EMF constant. Usually, the damping coefficient (B) is treated as like the load torque (T_L) with the rotor mechanical speed. So, if we assume the damping coefficient can be ignored, we can simplify the transfer function like (5.8). The transfer function (Eq. 5.8) provides insight into the motor's dynamic response to voltage changes. The denominator of the transfer function is a standard second-order system characteristic equation. It can be written in the form:

$$s^2 + \frac{R_a}{L_a}s + \frac{K^2}{J\,L_a} = s^2 + \frac{1}{\tau_e}s + \frac{1}{\tau_e \tau_m} \tag{5.9}$$

Where $\tau_e = L_a/R_a$ represents the electrical time constant, and $\tau_m = JR_a/K^2$ means the electro-mechanical time constant. Therefore, the poles of the transfer function can be calculated by

$$Pole_{1,2} = -\frac{1}{2\,\tau_e} \pm \frac{1}{\tau_e}\sqrt{\frac{1}{4} - \frac{\tau_e}{\tau_m}}, or\ Pole_{1,2} = -\frac{1}{2\,\tau_e} \pm j\frac{1}{\tau_e}\sqrt{\frac{\tau_e}{\tau_m} - \frac{1}{4}} \qquad (5.10)$$

The response characteristics of a motor's speed to armature voltage changes (Under-Damping, Critical Damping, Over-Damping) are determined by the ratio of the electrical time constant to the electromechanical time constant.

When the electrical time constant is large (high L_a, low R_a) and the electro-mechanical time constant is small (low J, high K), the motor's speed response tends to be oscillatory. This results in under-damping, where the system experiences oscillations before settling to the desired speed.

B. Controller design of the motor system

A proportional-integral (PI) controller is a fundamental component in motor control systems, complementing the dynamics influenced by the electrical and electromechanical time constants discussed earlier [92-95].

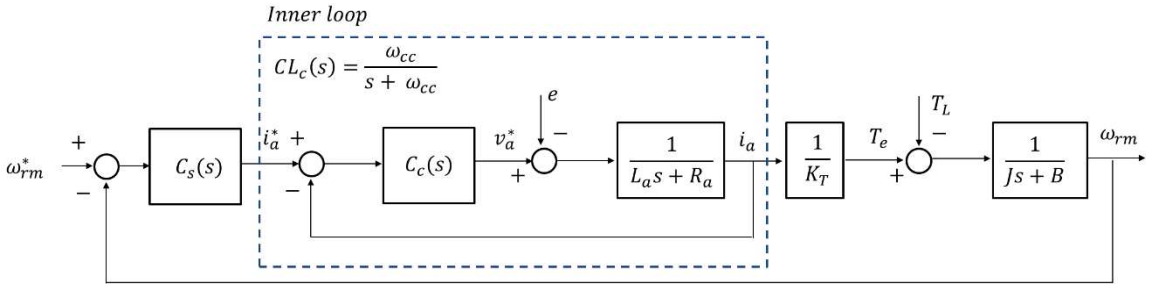


Figure 5. 3. The basic cascade connection PI control structure for the motor drive system.

Typically, motor control systems feature a cascade-connected structure as depicted in Figure 5.3. This configuration simplifies the design of speed and current controllers.

Generally, the inner loop's bandwidth is designed to be 7 to 10 times larger than that of the outer loop. This approach assumes ideal characteristics for the inner loop to facilitate the design of the outer loop controller. In this context, the inner loop refers to the motor's current controller ($C_c(s)$), which requires a bandwidth 7 to 10 times higher compared to the speed controller ($C_c(s)$). Typically, the inner loop, $CL_c(s)$, is treated as a first-order time-delay element. Therefore, designing the current controller to exhibit characteristics similar to a first-order low-pass filter is common practice. This design strategy ensures effective coordination between the inner current control and the outer speed control loops, optimizing the overall performance and stability of the motor control system.

Here, the current controller can be designed as follows:

$$C_c(s) = K_{p.c} + \frac{K_{i.c}}{s} \tag{5.11}$$

In eq (5.11), $K_{p.c}$ and $K_{i.c}$ can be set as $L_a\omega_{cc}$ and $R_a\omega_{cc}$, respectively, to have a 1st order low pass filter with ω_{cc} bandwidth.

If the current controller is designed with ideal response characteristics as described above, the speed controller can effectively consider the current controller to have a gain close to 1, rendering it negligible in designing the speed controller.

$$C_s(s) = K_{p.s} + \frac{K_{i.s}}{s} \tag{5.12}$$

If the speed controller is designed as described in equation (5.12), the transfer function for the speed command (ω_{rm}^*) can be derived as follows.

$$\frac{\omega_{rm}(s)}{\omega_{rm}^*(s)} = \frac{\frac{K_T K_{p.s}}{J}s + \frac{K_T K_{i.s}}{J}}{s^2 + \frac{K_T K_{p.s}}{J}s + \frac{K_T K_{i.s}}{J}} \tag{5.13}$$

Due to the influence of the zero, even if the system is designed for over-damping, it cannot avoid overshoot and oscillatory responses.

An IP (Integral-Proportional) controller is a type of feedback controller that combines the integral and proportional actions to maintain control over a process variable [94-95]. It is similar to a PI (Proportional-Integral) controller but with the order of the actions reversed in the control algorithm. The IP controller can be used to remove the zero from the transfer function as follows:

$$\frac{\omega_{rm}(s)}{\omega_{rm}^{*}(s)} = \frac{\frac{K_T K_{i.s}}{J}}{s^2 + \frac{K_T K_{p.s}}{J} s + \frac{K_T K_{i.s}}{J}} \tag{5.14}$$

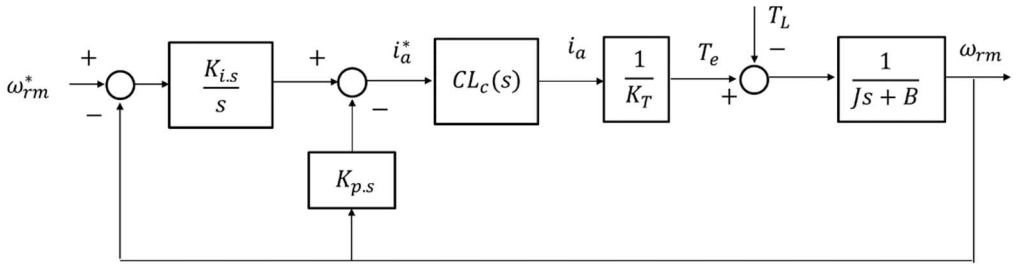


Figure 5. 4. The IP control structure for the motor drive system.

The IP controller effectively removes zero, which helps in reducing or eliminating overshoot and oscillatory responses. The system exhibits a more stable response with reduced oscillations. However, the IP controller is slower in response compared to the PI controller. Nevertheless, the primary focus of this study is the design of the current controller. Therefore, the IP controller is used here to minimize overshooting in the speed control, as like Figure 5.4.

5.1.2 Field Oriented Control (FOC) of the PMSM

In the previous section, we examined the DC motor control system. However, due to the power density limitations of DC motors, many industrial applications prefer three-phase AC motors. As mentioned earlier, this study focuses on permanent magnet synchronous motors (PMSMs). Three-phase AC motors can be controlled in a manner similar to DC

motors by using the d-q rotor synchronous reference frame, which simplifies the control process. Additional details on synchronous coordinate transformation can be found in Appendix A.

This section presents general control techniques for PMSMs. Field-Oriented Control (FOC) is a form of vector control [92-96]. The FOC method is a motor control strategy that specifies the direction of the stator current vector in the rotating reference frame of the machine. First, the general operating principles of FOC are introduced, followed by a detailed explanation of possible design methodologies.

The rotor position must be known to orient the rotor reference frame. The position is either measured with an encoder or estimated using a sensor-less technique. Three-phase AC voltage, current, and magnetic flux can be converted to the d-q synchronous coordinate system using this detected rotor position. A rotating reference frame's d and q axes have physical meanings in the context of an electrical machine. The d-axis is directly aligned with a rotor magnetic pole, while the q-axis is shifted by 90°E (electrical degrees), hence the quadrature axis. Two magnetic poles of opposite polarity are always shifted by 180°E. Therefore, based on the rotor position measured, the torque of the PMSM can be expressed as the cross-product of the flux vector (λ^e_{dqs}) and the current vector (i^e_{dqs}) in the e synchronous reference frame. The superscript e represents the synchronous reference frame.

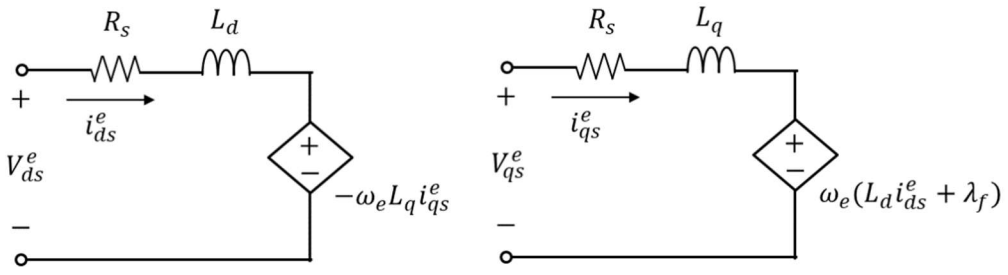
$$\boldsymbol{\lambda^e_{dqs}} = \begin{bmatrix}\lambda^e_{ds}\\ \lambda^e_{qs}\end{bmatrix} = \begin{bmatrix}L_d i^e_{ds} + \lambda_f\\ L_q i^e_{qs}\end{bmatrix}, \boldsymbol{i^e_{dqs}} = \begin{bmatrix}i^e_{ds}\\ i^e_{qs}\end{bmatrix} \tag{5.15}$$

$$T_e = \frac{3}{2}P\left(\boldsymbol{\lambda^e_{dqs}} \times \boldsymbol{i^e_{dqs}}\right) = \frac{3}{2}P\left\{\lambda_f i^e_{qs} + \left(L_d - L_q\right) i^e_{ds} i^e_{qs}\right\} \tag{5.16}$$

In general, the voltage equation of the permanent magnet synchronous motor (PMSM) is expressed in the rotor's d-q reference frame, as follows.

$$V^e_{ds} = R_s i^e_{ds} + L_d \frac{di^e_{ds}}{dt} - \omega_e L_q i^e_{qs} \tag{5.17}$$

$$V^e_{qs} = R_s i^e_{qs} + L_q \frac{di^e_{qs}}{dt} + \omega_e (L_d i^e_{ds} + \lambda_f) \tag{5.18}$$



(a) (b)

Figure 5. 5. The equivalent circuit of the PMSM in the rotor reference frame; (a) d-axis circuit, (b) q-axis circuit.

PMSMs are divided into Surface Permanent Magnet (SPM) and Interior Permanent Magnet (IPM) motors according to the permanent magnet arrangements on the rotor. In the case of SPM motors, it can be assumed that the inductances L_d and L_q are equal, ideally. Since the motor used in this study has L_d and L_q that almost match at the rated condition, it is assumed that $L_d = L_q = L_s$.

In this case, we can assume the magnet flux aligns with the d-axis, meaning the q-axis's flux is zero. Therefore, based on the Eq. (5.16), the torque can be re-written as follows.

$$T_e = \frac{3}{2} P \lambda_f i_{qs}^e \tag{5.19}$$

As a result, the current commands (i_{ds}^{e*}, i_{qs}^{e*}) from the torque command (T_e^*) can be expressed as follows except in the field weakening control area.

$$\begin{bmatrix} i_{ds}^{e*} \\ i_{qs}^{e*} \end{bmatrix} = \begin{bmatrix} 0 \\ \dfrac{T_e^*}{\frac{3}{2} P \lambda_f} \end{bmatrix} \tag{5.20}$$

Eq. (5.20) shows that the stator flux and torque can be controlled independently by the current i_{ds}^e and i_{qs}^e, respectively. In summary, the output of the speed PI or IP controller described in section 5.1.1 is transmitted as a torque command. Since the q-axis current command has a proportional relationship, as shown in Eq. (5.20), it can be calculated using

the above equation. For the d-axis, it is controlled to be zero, assuming $L_d = L_q$ and it is not within the field weakening control region.

These independently generated current commands are generally controlled using a PI controller separately. However, unlike a DC motor, a three-phase motor typically uses a feedforward compensation term $(V_{ff.d}, V_{ff.q})$ to offset the mutual interference term and the back electromotive force (EMF) term of the d-q synchronous coordinate system.

$$V_{ds}^{e*} = \left(K_{p.d} + \frac{K_{i.d}}{s}\right)(i_{ds}^{e*} - i_{ds}^{e}) + V_{ff.d} \tag{5.21}$$

$$V_{qs}^{e*} = \left(K_{p.q} + \frac{K_{i.q}}{s}\right)(i_{qs}^{e*} - i_{qs}^{e}) + V_{ff.q} \tag{5.22}$$

$$\boldsymbol{V_{ff}}(s) = \begin{bmatrix} V_{ff.d} \\ V_{ff.q} \end{bmatrix} = \begin{bmatrix} -\omega_e \widehat{L_q} i_{qs}^{e} \\ \omega_e (\widehat{L_d} i_{ds}^{e} + \widehat{\lambda_f}) \end{bmatrix} \tag{5.23}$$

Based on the above (5.21)~(5.23) equations, the current controller was then designed as shown in Figure 5.6, with the feedforward compensator. The carat symbol (^) appearing above the coefficient variables denotes the estimated parameters. Similarly, the star symbol $(*)$ above a value indicates it represents the desired value. From the pole-zero cancellation method, the control of the proportional gains $(K_{p.d}, K_{p.q})$ are set as $(\widehat{L_d}\omega_{cc}, \widehat{L_q}\omega_{cc})$, and the integral gains can be set as $(\widehat{R_s}\omega_{cc}, \widehat{R_s}\omega_{cc})$,

To avoid overvoltage error, an anti-windup limiter is included to limit the output voltage, with control gains $(K_{a.d}, K_{a.q})$. These anti-windup gains can set as $(1/K_{p.d}, 1/K_{p.q})$, according to Appendix. B [97].

So far, we have explored Field-Oriented Control (FOC), a widely used method in PMSM drive systems. In summary, FOC utilizes either a rotor position sensor or sensor-less techniques to align the d-axis with the motor's magnetic flux axis and controls the motor torque using the q-axis current. Based on this principle, we have also examined the design of controllers capable of regulating motor currents.

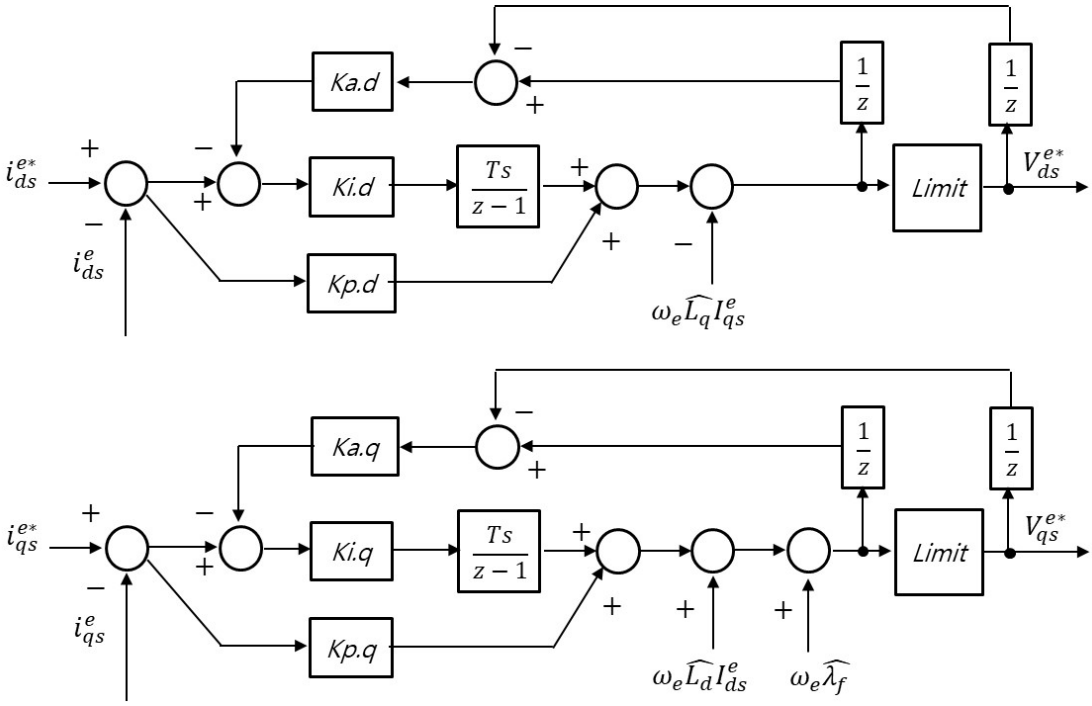


Figure 5. 6. Control block diagram of the digital PI controller for the d-q current with anti-windup.

The controllers discussed thus far are typically applied in conventional VSIs. However, the design of current controllers is different when considering CSIs.

5.2 AC Current Sensor-less Control design for All-SiC-based Buck-Current Source Inverter with PMSM

The Current Source Inverter causes resonant frequency due to the filter capacitor connected to the output terminal. Previously, the Proportional and Resonant (PR) controller or the multi-nested-loop controller was proposed to control the LC resonant frequency. Since system parameter errors heavily influence these controllers, complex vector controllers and Active Damping Control Methods using two-stage modeling of CSI-fed PMSM systems have been studied to improve response performance in previous studies [98-99].

Recently, as high-speed switching became possible through the application of the Wide-Band Gap switch, a method for simplifying and robust controller design was proposed [100]. In particular, the multi-loop-nested controller required the voltage sensor of the filter capacitor and AC current sensors. However, in recent research, it was possible to design a controller using only current sensors without additional voltage sensors.

On the other hand, current sensors are generally more expensive than voltage sensors and occupy a slightly larger volume in power electronics. In the case of Voltage Source Inverters, methods of reducing the number of current sensors using DC-Link current sensing have been widely proposed. Therefore, this study proposes a design method that simplifies the controller by using only the voltage sensor of the filter capacitor instead of load-side AC current sensors.

5.2.1 System Description

Compared to the VSI, the CSI plant model is more complex due to the presence of a filter capacitor, as illustrated in Figure 5.7. As illustrated in Figure 5.7, C_f is the output filter capacitor, e is the machine back electro-motive force, L_s the stator inductance, and

R_s the stator resistance. Since the current generated by the CSI is split between the motor current and the filter capacitor current, this relationship can be summarized by Eq. (5.24).

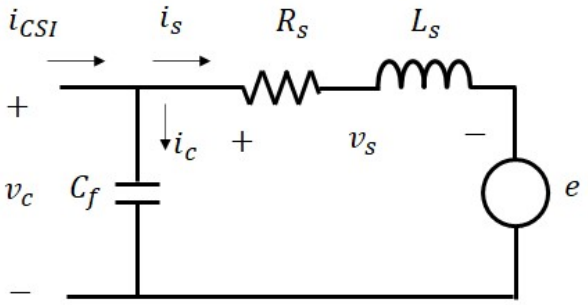


Figure 5. 7. Equivalent circuit of the CSI-fed motor in a stationary reference frame

$$i_{CSI} = i_s + i_c. \tag{5.24}$$

$$i_c = C_f \frac{dv_c}{dt}, and\ v_c = v_s + e. \tag{5.25}$$

$$v_c = L_s \frac{di_s}{dt} + R_s i_s + e \tag{5.26}$$

Equation (5.25) summarizes the filter capacitor current based on the capacitor voltage equation and Kirchhoff's voltage law. Additionally, the motor voltage equation can be expressed as shown in Equation (5.26). Based on this, the model can be organized into a two-stage system, as illustrated in Figure 5.8.

Due to the complexity of the equivalent circuit, the system characteristics of the CSI with PMSM can be analyzed using two-stage modeling, as shown in Figure 5.8 [98-99].

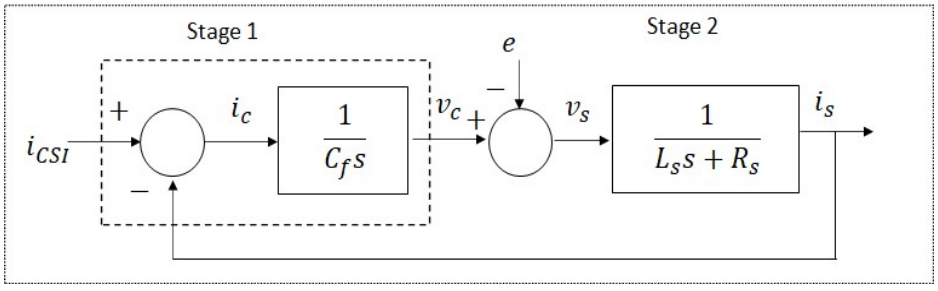


Figure 5. 8. Block diagram of CSI-fed PMSM in a stationary reference frame

Here, we denote the transfer functions of the filter capacitor and the motor plant as $G_1(s)$ and $G_2(s)$ respectively, as follows:

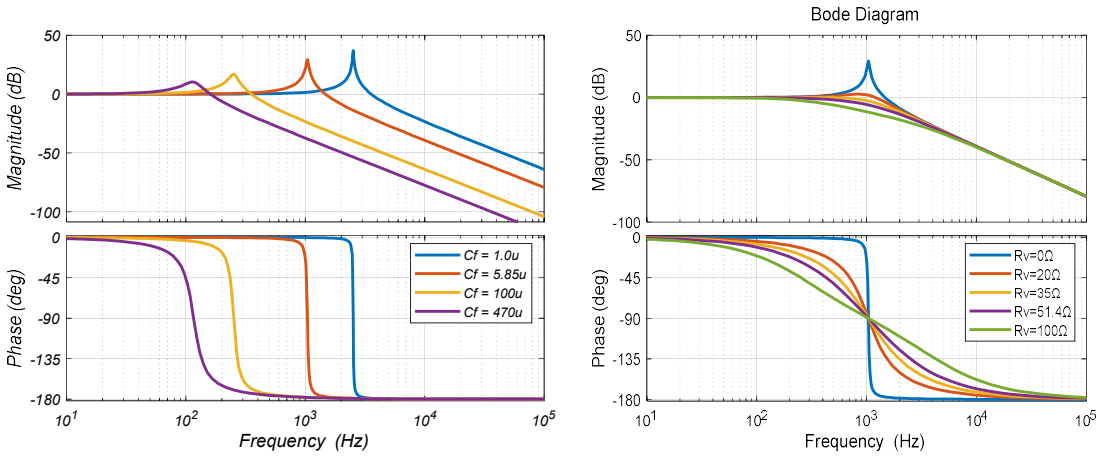
$$G_1(s) = \frac{1}{C_f s} \tag{5.27}$$

$$G_2(s) = \frac{1}{L_s s + R_s} \tag{5.28}$$

From Eq. (5.27) and (5.28), the motor current and the CSI current can be summarized as the following.

$$G_p(s) = \frac{i_s(s)}{i_{CSI}(s)} = \frac{1}{1 + G_1(s)G_2(s)} = \frac{\frac{1}{L_s C_f}}{s^2 + s\frac{R_s}{L_s} + \frac{1}{L_s C_f}} \tag{5.30}$$

Therefore, the transfer function of the CSI can be represented by a second-order system. According to Appendix. C [101], due to the motor inductance (L_s) and filter capacitor (C_f), a resonance frequency is formed. While the motor stator resistance (R_s), which acts as a damping coefficient (ζ), can attenuate this resonance if it is sufficiently large, a high physical winding resistance results in significant system losses.



(a) (b)

Figure 5. 9. The bode plot for the plant of current source inverter with PMSM, (a) depending on the output filter capacitance C_f , (b) depending on the stator resistance R_s.

In (5.31), Δv_{max} is the maximum tolerable output voltage ripple of the capacitor, I_{dc} represents the dc link current and f_{pwm} is the switching frequency of CSI. Moreover, motor current control requires a bandwidth that is 7 to 10 times higher than that of speed control, as explained in Section 5.1.1. For traditional IGBTs or Si-based MOSFETs, significant filter capacitance is needed due to the lower switching frequency. Depending on hardware design requirements, the capacitor size can be approximately considered based on Eq. (5.31) with the switching frequency [102].

$$C_f = \frac{I_{dc}}{4\,\Delta v_{c.max}\, f_{pwm}} \tag{5.31}$$

Therefore, as shown in Figure 5.9(a), if increasing the switching frequency is difficult, resulting in the larger filter capacitance, the resonance frequency will decrease. This necessitates designing a controller that can increase the bandwidth of the current controller. Additionally, as illustrated in Figure 5.9(b), increasing the motor stator resistance can attenuate the resonance response.

5.2.2 Conventional Current Controller in stationary reference frame.

To control a plant with two stages, a cascade controller with nested control loops is generally constructed. In Stage 1, as shown in Figure 5.8, the objective is to control the current of the capacitor so that the voltage reaches the desired value. The relationship between the voltage and current of the capacitor can be expressed as follows:

$$i_c = sC_f V_s \;\rightarrow V_s = \frac{1}{sC_f} I_c. \tag{5.32}$$

Since there is no pole in the plant, it is possible to design a proportional controller.

$$I_c^* = K_{pv}(V_s^* - V_s). \tag{5.33}$$

$$sC_f V_s = K_{pv}(V_s^* - V_s). \tag{5.34}$$

If we assume that the target current in equation (5.33) is equal to the steady-state current in equation (5.32), we can rearrange it as shown in equation (5.34). Using this, the relationship between the target voltage (V_s^*) and the response voltage (V_s) can be expressed as in equation (5.35). In this case, the controller gain (K_{pv}) can be designed as the product of the estimated filter capacitance ($\widehat{C_f}$) and the cut-off frequency (ω_f). If there is no error in the estimated capacitance, we can achieve a response characteristic similar to that of a first-order low pass filter, as shown in equation (5.36).

$$V_s = \frac{\frac{K_{pv}}{C_f}}{s + \frac{K_{pv}}{C_f}} V_s^*, \qquad K_{pv} = \widehat{C_f}\omega_f. \tag{5.35}$$

$$V_s = \frac{\omega_f}{s + \omega_f} V_s^*. \tag{5.36}$$

In Stage 2, similar to the traditional RL load, a PI controller can be used to design the controller as follows. First, the voltage equation applied to the load can be derived through Laplace transformation, as shown in equation (5.37). If the target voltage of the PI controller in equation (5.38) is equal to the voltage of the voltage equation in (5.37) at the steady state, it can be combined with the response of the Stage 1 controller in equation (5.36) and rearranged as shown in equation (5.39).

$$v_s = L_s \frac{di_s}{dt} + R_s i_s \;\; \rightarrow V_s = (sL_s + R_s) I_s \tag{5.37}$$

$$V_s^* = \frac{K_p s + K_i}{s} (I_s^* - I_s) \tag{5.38}$$

$$(sL_s + R_s) I_s = \frac{\omega_f}{s + \omega_f} \frac{K_p s + K_i}{s} (I_s^* - I_s) \tag{5.39}$$

$$I_s = \frac{\left(s\widehat{L_s} + \widehat{R_s}\right) \omega_f \omega_{cc}}{s(sL_s + R_s)\left(s + \omega_f\right) + (sL_s + R_s)\omega_f \omega_{cc}} I_s^* \tag{5.40}$$

If the PI gain ($K_p,\ K_i$) are set as ($\widehat{L_s}\ \omega_{cc}, \widehat{R_s}\ \omega_{cc}$) respectively, the transfer function can be induced as (5.40) where the estimated parameters (hat) are well matched. Simplifying this yields equation (5.41).

$$CL(s) = \frac{I_s}{I_s^*} = \frac{\omega_f\ \omega_{cc}}{s^2 + \omega_f s + \omega_f\ \omega_{cc}} \tag{5.41}$$

The designed controller can achieve the response characteristic equivalent to a second-order low pass filter by appropriately designing the cutoff frequency. The final designed control diagram is shown in Figure 5.10.

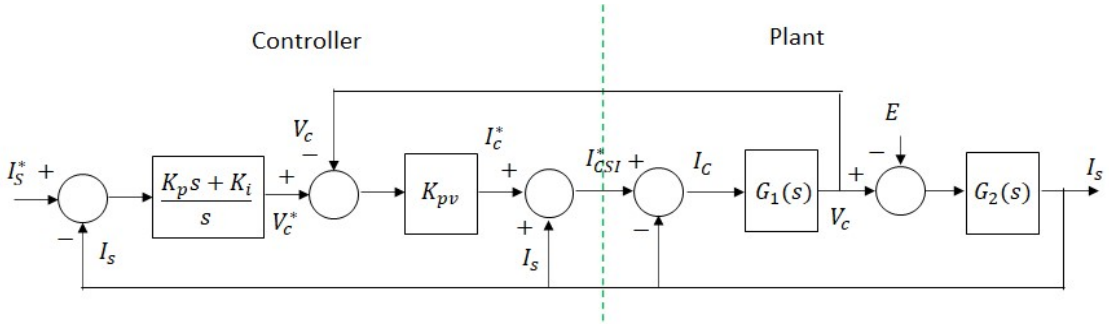


Figure 5. 10. The conventional multiple-nested-loop control design of CSI-fed PMSM.

This conventional controller needs to use two types of sensors. One of them is ac current sensor, and another one is voltage sensor

5.2.3 AC current sensor-less Current Controller Design in stationary reference frame.

The current controller proposed in this study is closely related to the capacitance of the filter capacitor. By increasing the switching frequency, the capacitance can be reduced, achieving sufficient bandwidth for current control as shown in the Bode plot in Figure 5.9(a). Implementing a virtual resistor in the controller can increase the damping resistance, resulting in a damped response with a wide control bandwidth, as depicted in Figure 5.9(b).

The CSI has an intrinsic characteristic of nearly 0 dB gain at lower frequencies, less than approximately 0.3 $f_{resonant}$. Thus, when the resonance response is reduced, the output current of the CSI and the input current of the load become nearly equal (i.e., $I_{CSI} \approx I_s$ @ $< 0.3\ f_{resonant}$) [100].

The main concept is to significantly raise the switching frequency using SiC MOSFETs, setting the resonance frequency above the required control band for AC load control. Since the output current of the CSI matches the load current, it becomes possible to implement a virtual damping resistance through a digital controller utilizing voltage detection across the filter capacitor, eliminating the need for current sensors on the AC load.

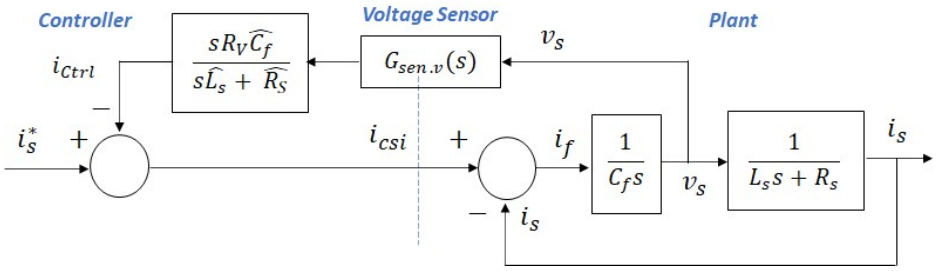


Figure 5. 11. The proposed ac-current sensor-less controller.

The block diagram depicted in Figure 5.11 represents an ideal implementation of the virtual resistance in a CSI drive, eliminating the need for an AC current sensor. In this figure, $\widehat{C_f}$ represents the estimated filter capacitance, $\widehat{L_s}$ is the estimated load inductance

(motor phase inductance), and $\widehat{R_s}$ denotes the load resistance (motor phase resistance) [7, 8]. The proposed controller can be designed as follows, which uses the capacitor voltage information as input to compensate the control quantity (I_{Ctrl}) to achieve the target current (I_s^*).

$$C(s) = \frac{I_{Ctrl}(s)}{V_S(s)} = \frac{sR_V\widehat{C_f}}{s\widehat{L_s} + \widehat{R_S}} = \frac{\frac{sR_V\widehat{C_f}}{\widehat{L_s}}}{s + \frac{\widehat{R_S}}{\widehat{L_s}}} \tag{5.42}$$

From Eq. (5.27) and (5.28), the closed-loop transfer function can be derived as follows.

$$CL(s) = \frac{I_S(s)}{I_S^*(s)} = \frac{\frac{G_1(s)\,G_2(s)}{1 + G_1(s)\,C(s)}}{1 + \frac{G_1(s)G_2(s)}{1 + G_1(s)\,C(s)}} = \frac{\frac{1}{L_sC_f}}{s^2 + s\frac{(R_s + R_V)}{L_s} + \frac{1}{L_sC_f}} \tag{5.43}$$

A second-order system incorporating a virtual damping resistance can be derived using the formulas derived equations (5.42) to (5.43) in the continuous time domain. I_s^* represents a desired target current in (5.43). In order to obtain the fastest response corresponded to the critically damped system that contains no overshooting, the pole locations of the second-order system can be designed like this.

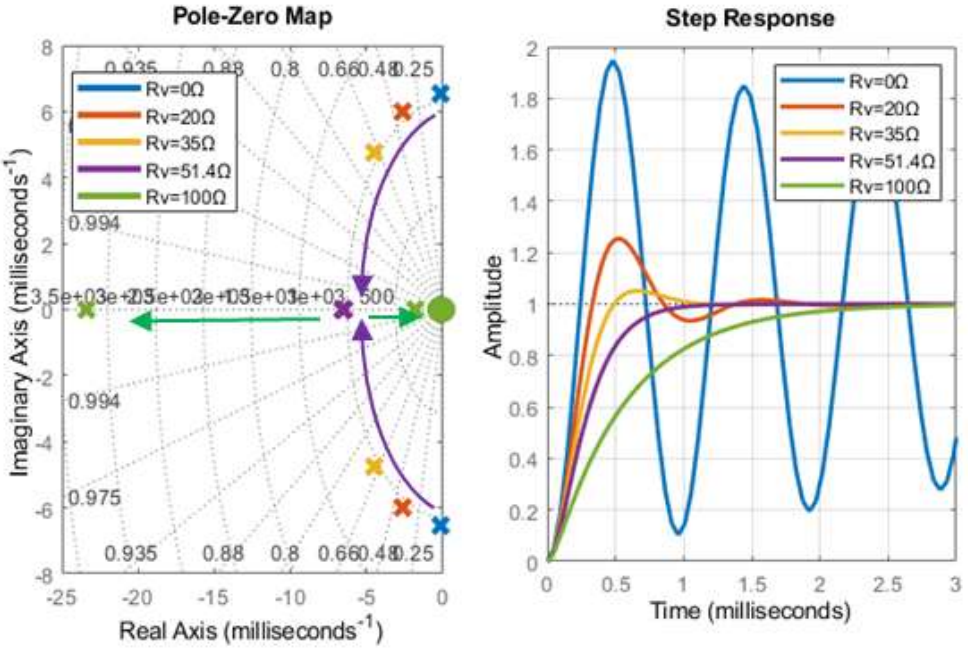
$$Pole = -\frac{R_v + R_s}{2L_s} \pm \frac{1}{2}\sqrt{\frac{(R_v + R_s)^2}{L_s^2} - \frac{4}{L_sC_f}} \tag{5.44}$$

$$\frac{(R_v + R_s)^2}{L_s^2} - \frac{4}{L_sC_f} = 0\,, \quad R_v + R_s = 2\sqrt{\frac{L_s}{C_f}} \tag{5.45}$$

If the motor inductance (L_s) is 4mH, the filter capacitance (C_f) is 5.85μF, and the motor stator resistance (R_s) is 0.9 ohms, the control gain (R_v) for achieving a critically damped response is calculated to be 51.4 ohms.

Figure 5.12 shows the step response and the migration of the poles/zeros of the closed-loop transfer function $CL(s)$ when varying the virtual resistance. As shown in Figure 5.12(a), when the designed control gain $R_v = 51.4$, the pole reaches the real axis of the left

half-plane, resulting in a critically damped response. This critically damped response is confirmed by the purple graph in Figure 5.12(b).



(a) (b)

Figure 5. 12. (a) the pole-zero map according to the series connected virtual resistance in closed-loop transfer function, (b) unit step response depending on the virtual resistance in closed-loop transfer function.

The controller designed in continuous time must be implemented in a digital controller. Figure 5.13 illustrates the proposed controller in discrete time. The computed control values are output by the CSI through PWM, during which a time delay occurs [100,103].

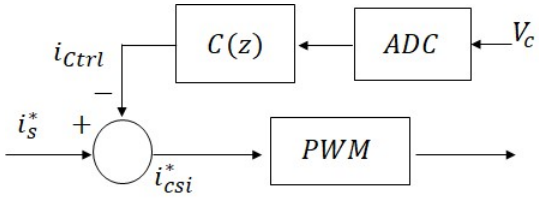


Figure 5. 13. Discrete time domain block diagram of the CSI-AC load drive with virtual resistance feedback in stationary reference frame.

To design the controller in the discrete time domain, the z-transformation was performed using the Zero-Order Hold (ZOH) method, as follows.

$$C(z) = (1 - z^{-1})Z\left\{\frac{C(s)}{s}\right\} = \frac{\frac{R_V \widehat{C_f}}{\widehat{L_s}}(z-1)}{z - e^{-\frac{\widehat{R_s}}{\widehat{L_s}}T_s}} \tag{5.46}$$

Here, T_s is sampling time. Typically, the sampling frequency of conventional motor controllers is within 10-20kHz. However, when using WBG power switches, the increase in switching frequency necessitates a corresponding increase in the sampling frequency for control purposes. This increase provides significant advantages in discrete time.

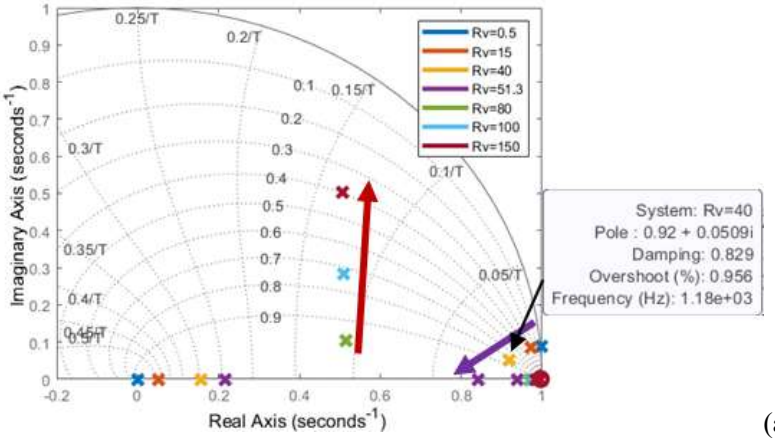
As mentioned earlier, the implementation of PWM introduces the time delay. If a unit time delay occurs first, the closed-loop transfer function can be obtained as follows.

$$G_1(z) = \frac{\frac{T_s}{C_f}}{z-1}, \quad G_2(z) = \frac{1}{R_s}\frac{1 - e^{-\frac{R_s}{L_s}T_s}}{z - e^{-\frac{R_s}{L_s}T_s}} \tag{5.47}$$

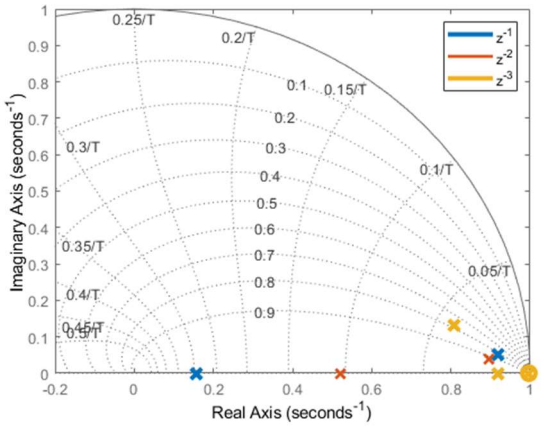
$$CL(z) = \frac{z^{-1}\, G_1(z)\, G_2(z)}{1 + z^{-1}\, G_1(z)\, C(z) + z^{-1} G_1(z) G_2(z)} \tag{5.48}$$

Figure 5.14 shows the various pole locations of the closed-loop transfer function CL(z). Due to symmetry with respect to the real axis, only the first and second quadrants are displayed. The sampling frequency is set to 75 kHz. Before discussing the analysis results, it should be noted that, in the discrete domain, poles closer to the point (1,0) are dominant and exhibit slower dynamic behavior. Therefore, the analysis below primarily focuses on these poles. The dashed reference lines in the z-grid indicate the damping factor and the natural frequencies of the poles.

Figure 5.14(a) illustrates the changes in pole locations for various virtual resistance values. The calculated $R_v = 51.3\ \Omega$ in the continuous time domain causes the real pole to move toward +1, slowing the response. Therefore, from this graph, $R_v = 40\ \Omega$ can be considered the optimal value for the system's damping factor of approximately 0.8. Values higher or lower than this cause oscillations or system delays.

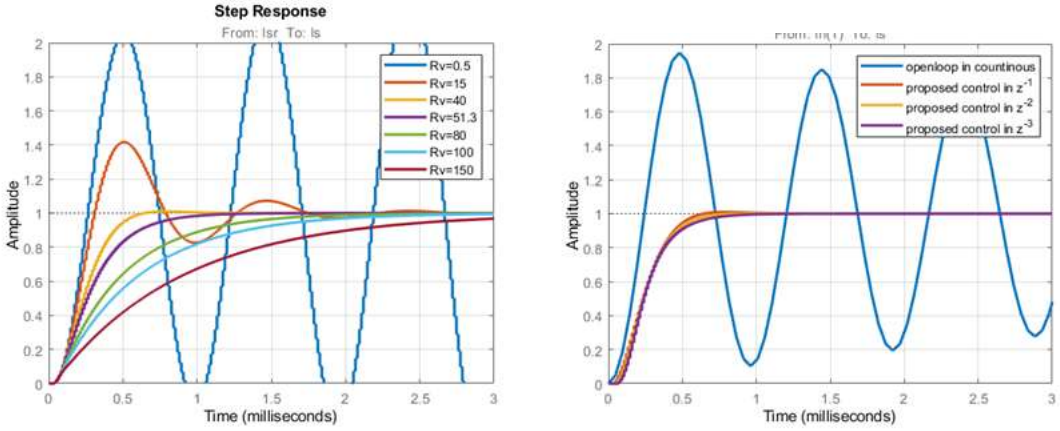


(a)



(b)

Figure 5. 14. Poles migration of the closed-loop transfer function CL(z) when varying, (a) virtual resistance R_v; (b) feedback loop delay ($R_v = 40\Omega$).



(a) (b)

Figure 5. 15. step response of the CSI motor drive comparing the transfer function of an open-loop system with closed-loop systems with proposed controller (a) when virtual resistance varying (b) when feedback delay varying.

The second parameter analyzed in Figure 5.14(b) is the feedback delay. Initially, the optimal gain was selected under the assumption of only unit delay. Maintaining the selected $R_v = 40\ \Omega$, additional feedback loop delays were assumed. The analysis shows that up to 2 sample delays result in response delays, and delays exceeding 3 sample periods start to induce oscillations.

Using the selected virtual resistance in the discrete-time domain, the damped resonance response can be observed in the closed-loop response shown in Figure 5.15(a). Even with a feedback delay, up to 3 samples did not significantly cause delay or induce oscillations. The corresponding step response curve can be seen in Figure 5.15(b).

5.2.4 AC current sensor-less Current Controller Design in *e* synchronous reference frame.

The AC machine drive system, fed by a Current Source Inverter (CSI), can be modeled in the synchronous reference frame using equations (5.49)-(5.51). To capture the behavior of machines like Permanent Magnet Synchronous Machines (PMSM) or Synchronous Reluctance Machines, the voltage and current equations of the AC machine are employed for modeling from Figure 5.16.

$$\begin{bmatrix} i_{di}^e \\ i_{qi}^e \end{bmatrix} = \begin{bmatrix} i_{ds}^e \\ i_{qs}^e \end{bmatrix} + \begin{bmatrix} i_{dc}^e \\ i_{qc}^e \end{bmatrix}. \tag{5.49}$$

$$\begin{bmatrix} i_{dc}^e \\ i_{qc}^e \end{bmatrix} = \begin{bmatrix} \rho C_f & -\omega_e C_f \\ \omega_e C_f & \rho C_f \end{bmatrix} \begin{bmatrix} v_{dc}^e \\ v_{qc}^e \end{bmatrix}. \tag{5.50}$$

$$\begin{bmatrix} v_{dc}^e \\ v_{qc}^e \end{bmatrix} = \begin{bmatrix} R_s + \rho L_{ds} & -\omega_e L_{qs} \\ \omega_e L_{ds} & R_s + \rho L_{qs} \end{bmatrix} \begin{bmatrix} i_{ds}^e \\ i_{qs}^e \end{bmatrix} + \begin{bmatrix} e_{ds}^e \\ e_{qs}^e \end{bmatrix}. \tag{5.51}$$

where i_{dqi}^e are d- and q-axes output current of a CSI, i_{dqs}^e denotes d- and q-axes stator current of an ac machine, i_{dqc}^e denotes d- and q-axes stator current of an output filter capacitor, v_{dqc}^e represent d- and q-axes voltage of an output filter capacitor, C_f is an output

filter capacitor of a CSI, R_s is a stator resistance of an ac machine, L_{dqs} are d- and q-axes synchronous inductance of an ac machine, ω_e represents a synchronous angular speed of an ac machine, e^e_{dqs} denote a back-emf voltage of an ac machine, and ρ is a differential operator i.e. d/dt. And superscripts "s" and "e" denote stationary and synchronous reference frame.

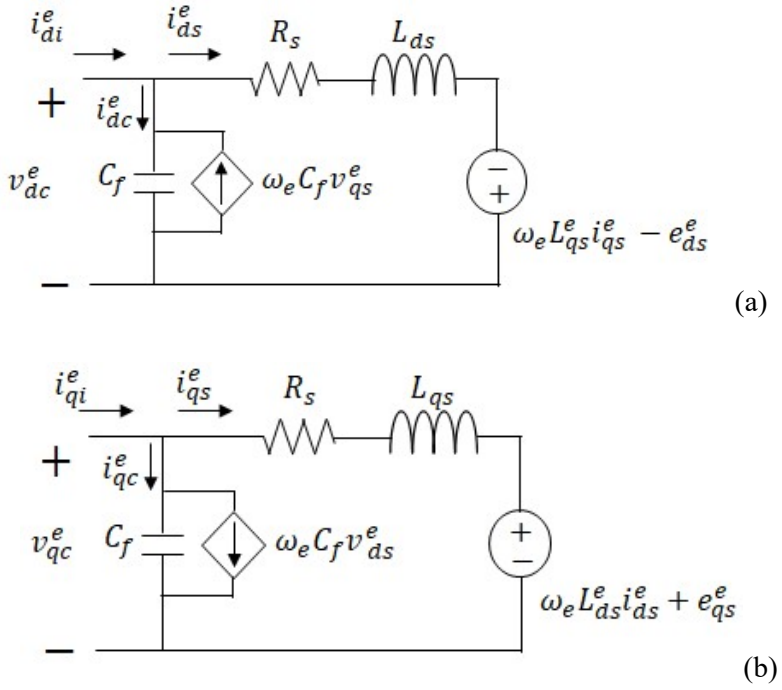


Figure 5. 16. The equivalent circuit of a Current Source Inverter (CSI) incorporating the AC motor system and capacitor filter can be represented in the e synchronous reference frame. (a) d-axis equivalent circuit. (b) q-axis equivalent circuit.

Our ultimate objective is to apply the controller to a three-phase motor system. To achieve this, the designed controller in the stationary reference frame can be extended by utilizing the e synchronous reference frame. The desired system response in the synchronous reference frame can be summarized as described in equation.

$$\begin{bmatrix} i^e_{ds} \\ i^e_{qs} \end{bmatrix} = \begin{bmatrix} \frac{\frac{1}{C_f L_{ds}}}{\rho^2 + \rho\frac{(R_s+R_{vd})}{L_{ds}} + \frac{1}{C_f L_{ds}}} & 0 \\ 0 & \frac{\frac{1}{C_f L_{qs}}}{\rho^2 + \rho\frac{(R_s+R_{vq})}{L_{qs}} + \frac{1}{C_f L_{qs}}} \end{bmatrix} \begin{bmatrix} i^{e*}_{ds} + i^e_{dctrl} \\ i^{e*}_{qs} + i^e_{qctrl} \end{bmatrix} \tag{5.52}$$

R_{vd} and R_{vq} are the d- and q-axes virtual resistance, respectively. $i^e_{dq.ctrl}$ denotes the controller and i^{e*}_{dqs} denotes the desired target current. To achieve the desired response like (5.52), the controller has to compensate the coupling term of the d-q synchronous reference frame.

$$\begin{bmatrix} i^e_{dc} \\ i^e_{qc} \end{bmatrix} = \begin{bmatrix} sC_f & 0 \\ 0 & sC_f \end{bmatrix} \begin{bmatrix} v^e_{dc} \\ v^e_{qc} \end{bmatrix} + \begin{bmatrix} 0 & -\omega_e C_f \\ \omega_e C_f & 0 \end{bmatrix} \begin{bmatrix} v^e_{dc} \\ v^e_{qc} \end{bmatrix} = \begin{bmatrix} sC_f & 0 \\ 0 & sC_f \end{bmatrix} \begin{bmatrix} v^e_{dc} \\ v^e_{qc} \end{bmatrix} + \begin{bmatrix} v^e_{dc.ff} \\ v^e_{qc.ff} \end{bmatrix} \tag{5.53}$$

$$\begin{bmatrix} v^e_{dc.ff} \\ v^e_{qc.ff} \end{bmatrix} = \begin{bmatrix} 0 & -\omega_e \widehat{C_f} \\ \omega_e \widehat{C_f} & 0 \end{bmatrix} \begin{bmatrix} v^e_{dc} \\ v^e_{qc} \end{bmatrix} \tag{5.54}$$

From (5.50), it is possible to separate the coupling term, as shown in equation (5.53). Furthermore, the decoupling method can be accomplished by utilizing the feed-forward compensator provided in equation (5.54). Additionally, by employing Equations (5.51) and (5.53), the system can be rearranged and organized as depicted in (5.55). Furthermore, utilizing a feed-forward compensator, the relationship between the desired current and the resulting current, as illustrated in (5.52), can be controlled and organized as shown in (5.56).

$$\begin{bmatrix} i^e_{di} \\ i^e_{qi} \end{bmatrix} = \begin{bmatrix} i^e_{ds} \\ i^e_{qs} \end{bmatrix} + \begin{bmatrix} sC_f & 0 \\ 0 & sC_f \end{bmatrix} \begin{bmatrix} v^e_{dc} \\ v^e_{qc} \end{bmatrix} + \begin{bmatrix} v^e_{dc.ff} \\ v^e_{qc.ff} \end{bmatrix} \tag{5.55}$$

$$\begin{bmatrix} i^{e*}_{ds} \\ i^{e*}_{qs} \end{bmatrix} = \begin{bmatrix} i^e_{di} \\ i^e_{qi} \end{bmatrix} - \begin{bmatrix} i^e_{d.ctrl} \\ i^e_{q.ctrl} \end{bmatrix} - \begin{bmatrix} v^e_{dc.ff} \\ v^e_{qc.ff} \end{bmatrix} \tag{5.56}$$

$$\begin{bmatrix} i^{e*}_{ds} \\ i^{e*}_{qs} \end{bmatrix} = \begin{bmatrix} 1 + sC_f R_s + s^2 L_{ds} C_f & -sC_f \omega_e L_{qs} \\ sC_f \omega_e L_{ds} & 1 + sC_f R_s + s^2 C_f L_{qs} \end{bmatrix} \begin{bmatrix} i^e_{ds} \\ i^e_{qs} \end{bmatrix} + \begin{bmatrix} sC_f & 0 \\ 0 & sC_f \end{bmatrix} \begin{bmatrix} e^e_{ds} \\ e^e_{qs} \end{bmatrix} - \begin{bmatrix} i^e_{d.ctrl} \\ i^e_{q.ctrl} \end{bmatrix} \tag{5.57}$$

When the d-q coupling of the filter capacitor is effectively compensated using the feed-forward compensator, the system can be arranged as illustrated in (5.57). In

most cases, the induced voltage of the motor, represented by e^e_{dqs}, does not exhibit significant changes due to mechanical inertia during high-speed sampling. As a result, it can be disregarded. Consequently, in the synchronous coordinate system, the current controller can be organized according to the representation shown in (5.58).

$$\begin{bmatrix} i^e_{d.ctrl} \\ i^e_{q.ctrl} \end{bmatrix} = \begin{bmatrix} \dfrac{-s\widehat{C_f}R_{vd}}{\widehat{R_s}+s\widehat{L_{ds}}} & 0 \\ 0 & \dfrac{-s\widehat{C_f}R_{vq}}{\widehat{R_s}+s\widehat{L_{qs}}} \end{bmatrix} \begin{bmatrix} v^e_{dc}-e^e_{ds} \\ v^e_{qc}-e^e_{qs} \end{bmatrix} + \begin{bmatrix} 0 & -\dfrac{s\widehat{C_f}\omega_e\widehat{L_{qs}}}{\widehat{R_s}+\omega_e\widehat{L_{qs}}} \\ \dfrac{s\widehat{C_f}\omega_e\widehat{L_{ds}}}{\widehat{R_s}+\omega_e\widehat{L_{ds}}} & 0 \end{bmatrix} \begin{bmatrix} v^e_{dc}-e^e_{ds} \\ v^e_{qc}-e^e_{qs} \end{bmatrix} \tag{5.58}$$

The decoupling term in equation (5.58) includes a derivative component that may introduce unstable from noise or other disturbances in the digital system. To address this issue, a digital filter was employed to mitigate the differential term, as illustrated in equation (5.59).

$$C_{PF}(z) = \frac{s}{s+\ \omega_c}\Big|_{s=\frac{2z-1}{Tz+1}} = \frac{z-1}{\left(1+\frac{\omega_c T_s}{2}\right)z-\left(1-\frac{\omega_c T_s}{2}\right)} \tag{5.59}$$

Consequently, the proposed digital controller can be structured as depicted in equation (5.60) [104].

$$\boldsymbol{C(z)} = \begin{bmatrix} \dfrac{R_{Vd}\widehat{C_f}}{\widehat{L_{ds}}}(z-1) & \dfrac{\widehat{C_f}\omega_e\widehat{L_{qs}}}{\widehat{R_s}+\omega_e\widehat{L_{qs}}}C_{PF}(z) \\ \dfrac{-\widehat{C_f}\omega_e\widehat{L_{ds}}}{\widehat{R_s}+\omega_e\widehat{L_{ds}}}C_{PF}(z) & \dfrac{\dfrac{R_{Vq}\widehat{C_f}}{\widehat{L_{qs}}}(z-1)}{z-e^{-\frac{\widehat{R_s}}{\widehat{L_{qs}}}T_s}} \end{bmatrix} \begin{bmatrix} v^e_{dc}-e^e_{ds} \\ v^e_{qc}-e^e_{qs} \end{bmatrix} \tag{5.60}$$

6. Proof-of-concept Demonstration

In this chapter, the prototypes developed based on the designs and concepts previously explained are introduced and validated.

First, a prototype of a three-phase Buck-CSI inverter utilizing commercial discrete SiC power switches is presented. This prototype is used to implement FPGA-based Space Vector Modulation, as introduced in Chapter 3, and to verify the power conversion efficiency of the CSI under switching frequency conditions exceeding 100kHz.

In Chapter 4, lightweight bidirectional switches based on IMS technology and high-temperature operable bidirectional switches using POL technology were designed. Prototypes of these two switch types were constructed, and their performance was validated through experiments in this chapter.

Finally, the simplified current controller proposed in Chapter 5, which operates without motor current sensors, was verified through an actual motor test bench.

6.1 Three-phase Current Source Inverter

A prototype was developed to verify the high efficiency and sinusoidal output voltage of a basic three-phase Current Source Inverter (CSI) with Space Vector PWM (SVPWM), as shown in Figure 6.1. The circuit design considered splitting the inductor into two parts to reduce its overall volume. Commercially available SiC MOSFETs were used in this design. This prototype was designed at TU Graz and tested at KUAS as part of collaboration with Mr. Riegler Benedikt and Prof. Michael Hartmann at TU Graz [105].

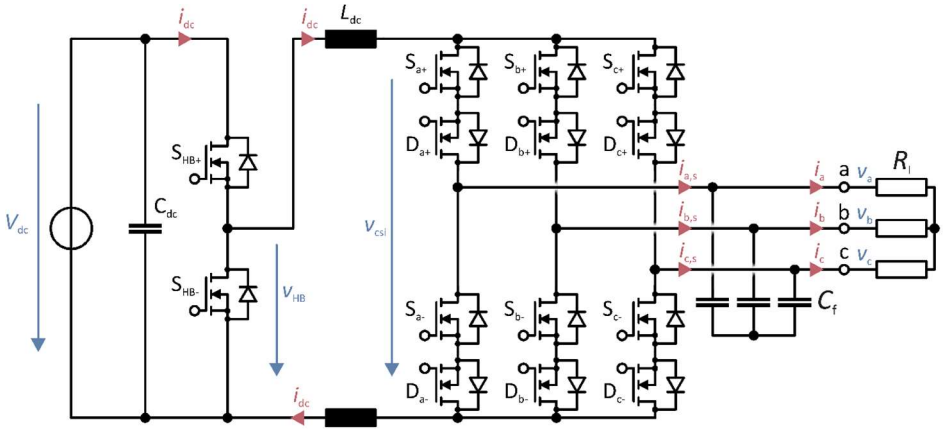


Figure 6. 1. Basic circuit diagram of the CSI with a buck input stage

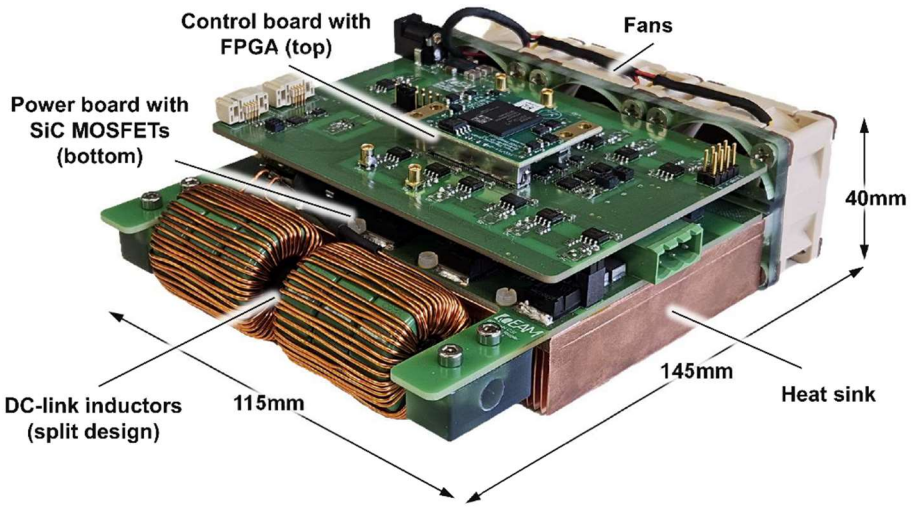
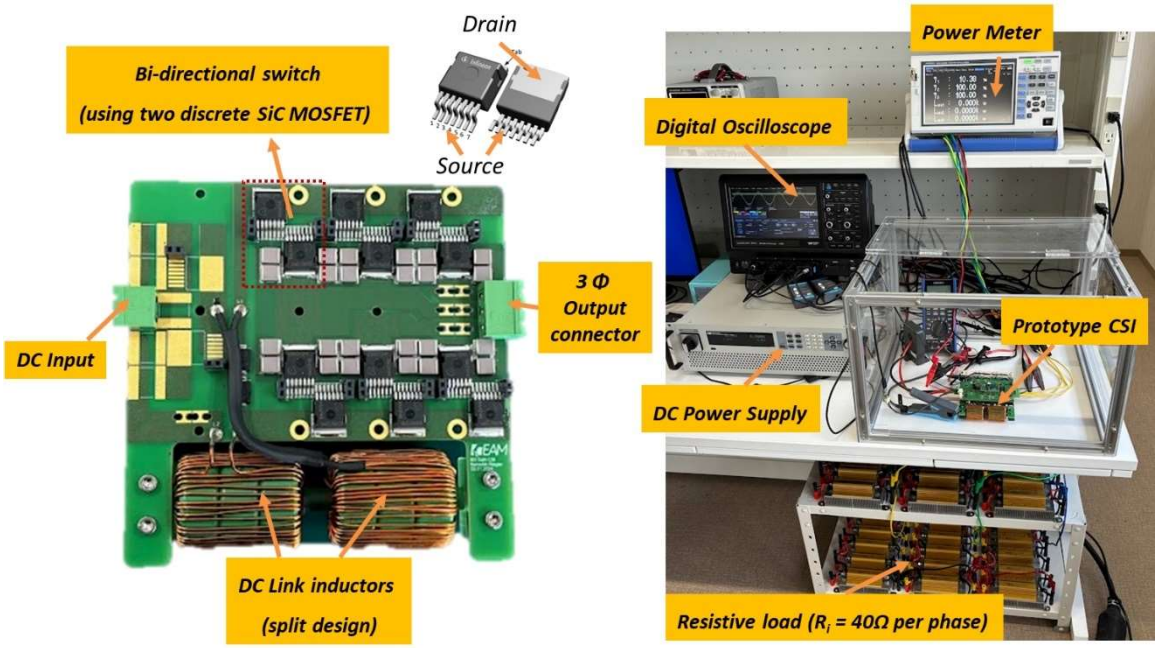


Figure 6. 2. Picture of the built buck-CSI prototype featuring a stacked two board design and an integrated thermal management system [105].

Figure 6.2 shows the prototype of the fabricated Buck-CSI. The control board containing the driver circuits for the SiC MOSFETs, the ADCs, and the FPGA are located on the top board. The SiC MOSFETs with the filter capacitors is located on the bottom board , as seen in Figure 6.3 (a).

Table 6. 1. Summary of the prototype specification

Parameter	*Symbol*	*Value*
Rated Output Power	P	3 kW
Rated output voltage	V_{rms}	200 V
Rated output current	I_{rms}	5 A
DC-link current	I_{dc}	8 A
Design switching frequency	f_{sw}	100 kHz
DC-link inductance	L_{dc}	1158 µH
Filter capacitance per phase	C_{f}	800 nF
Power Semiconductor Device Type	-	IMBG65R072M1HXTMA1
CSI overlap time	t_{ol}	40 ns



(a) (b)

Figure 6. 3. (a) The bottom board of Buck-CSI for SiC MOSFETs and filter capacitors with power pattern on the PCB, (b) resistive load test conditions [105]

The reverse blocking semiconductor switches are represented by MOSFETs in a back-to-back configuration, and the DC-link inductor is split between the positive and negative rail. The designed system has an output power of 3 kW with an RMS output voltage of 200 V, resulting in a DC-link current of approximately 7 A. The system's maximum DC input voltage is 500 V. The initial operating frequency for both the buck stage and the CSI was set at 100 kHz, with the potential for increasing this frequency. The prototype includes an FPGA-based control system, onboard ADCs, and an integrated thermal management system for the power semiconductor switches.

The main switching elements' reverse voltage blocking capability was achieved using a back-to-back configuration of two SiC MOSFETs in a compact SMD package (TO-263-7). The DC-link inductor employs a split toroidal design, as illustrated in Fig. 1. C0G-dielectric-based ceramic capacitors were used for the filter capacitors and were positioned as close as possible to the semiconductor switches to minimize the commutation loop area. A detailed summary of the prototype specifications is provided in Table 6.1.

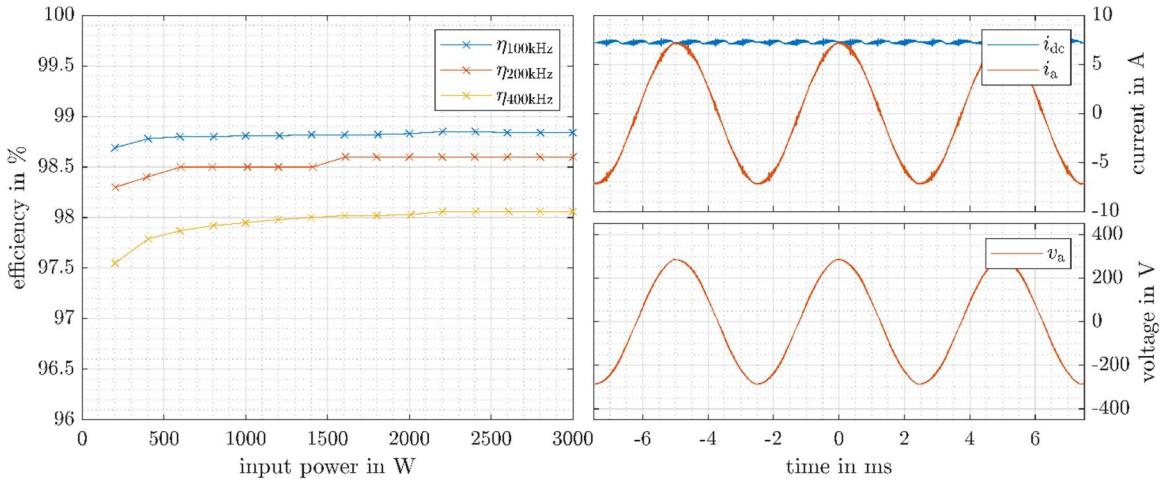


Figure 6. 4. (a) Measured converter efficiency over the entire load range at three different switching frequencies. (b) Measured DC-link current and output current and voltage of phase a at converter input power of 3 kW [105].

Efficiency measurements were conducted over the entire load range of the inverter, using a constant resistive load of $R_l = 40\Omega$ per phase. The converter's output power was

incrementally increased from 200 W to 3 kW in steps of 200 W by adjusting the DC-link current between 0 A and 7.5 A. The modulation index was kept constant at ($M = 1$), since the buck stage could vary the DC-link current based on load conditions and the AC output frequency, which was set at 200 Hz. Efficiency was measured at each increment using a power analyzer. The experiment was carried out at three different switching frequencies (100 kHz, 200 kHz, and 400 kHz), and the resulting efficiency curves are shown in Figure 6.4. Additionally, the measured output current and voltage in phase a, along with the DC-link current of the converter at the rated power of 3 kW, are displayed.

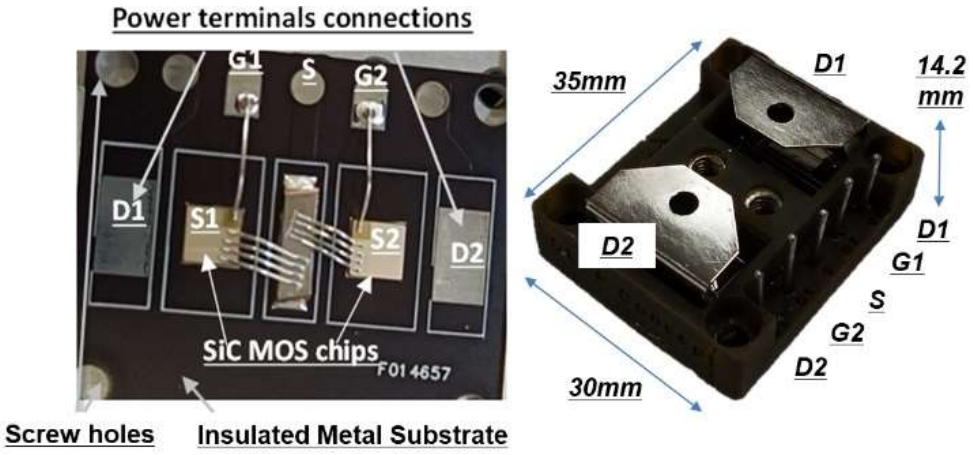
This result showcases a compact 3 kW current-source inverter prototype with a buck stage input that leverages all-SiC technology. The system operates at a high efficiency with a switching frequency of 400 kHz. The experimental findings confirm that the system meets or surpasses the design specifications.

6.2 Custom-designed power module

This section describes the prototypes of the two bidirectional switches designed in Chapter 4 and presents the results of validation tests conducted to assess their switching characteristics.

6.2.1 IMS-based bidirectional switch Prototyping and Validation

Figure illustrates the BDS prototype in detail. Part (a) provides an in-depth look at the internal structure, where the transistors are affixed by soldering on the drain side to the IMS tracks. For source and gate interconnections, ultrasonic bonding is utilized with bond-wires (labeled G for gate, S for source, and D for drain).



(a) (b)

Figure 6. 5. IMS-based bi-directional Switch prototype development: (a) detailed internal view, (b) external view.

In part Figure 6.5 (b), the assembly process is shown in three key steps. Firstly, the power terminals are mounted using a combination of soldering and ultrasonic bonding techniques, while the drive terminals are exclusively mounted by soldering. This dual approach enhances the durability and electrical performance of the connections. Secondly, the switch

is placed within a specially designed polymer housing, which is then filled with dielectric gel through designated apertures to provide insulation and protection against environmental factors. Finally, sealing taps are inserted to ensure a complete and secure enclosure, preventing any potential ingress of contaminants.

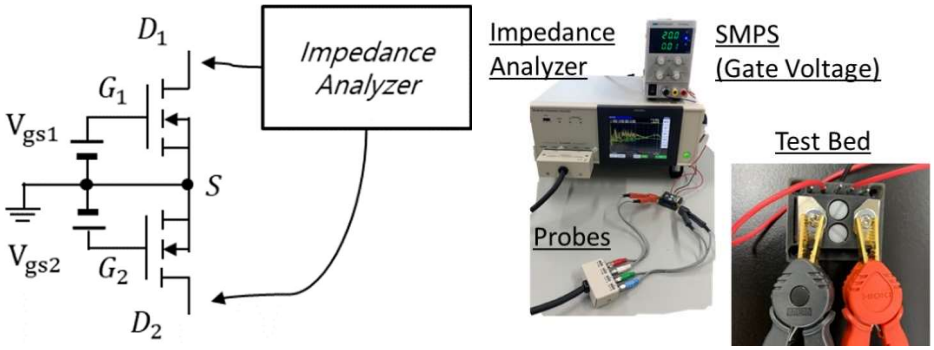
One of the well-known challenges associated with IMS technology, as opposed to ceramic substrates like direct bonded copper (DBC), is efficient heat extraction. This issue arises because IMS substrates do not dissipate heat as effectively as ceramic substrates. Therefore, it is crucial to mount the substrate securely to a cooling device to manage thermal performance effectively. In the case of aluminum substrates, as depicted in Figure 6.5, soldering onto a heatsink is not feasible. Instead, the substrate must be mounted using screws to ensure adequate thermal contact and stability. This method allows for effective heat dissipation while maintaining the integrity and performance of the power module.

Initially, a circuit resembling Figure 6.6(a) was assembled to assess the interconnection resistance and parasitic inductance of the prototype against simulation values. Employing a gate-source voltage of 20V for each power semiconductor, the impedance between D1 and D2 was gauged using HIOKI's impedance analyzer IM3670 and L2000 4-terminal Probe [106]. Measured data on inductance and resistance based on frequencies are presented in Figure 6.6(c). The utilization of screw bolts to secure the power terminal led to a slight elevation in the resistance value. Upon separate measurement, it was determined that the screw bolt contributed approximately 5mΩ. Taking this into account, it can be affirmed that the values closely align with the simulation results, as evidenced in Table 6.2, particularly at the considered switching frequency of 75 kHz [107-109].

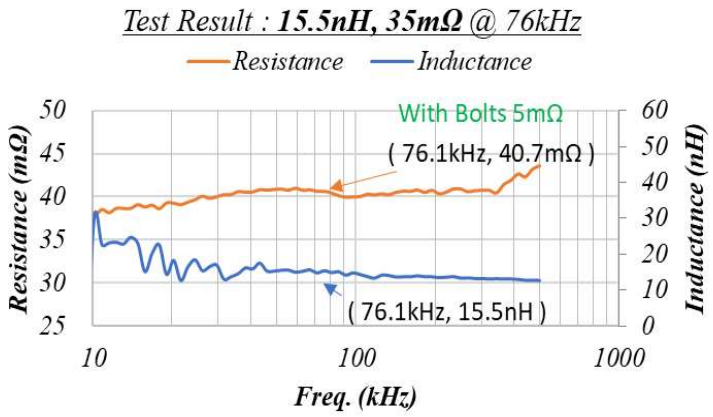
The designed BDS’s stray inductance, at approximation 15nH, does not exhibit significant differences compared to a SiC MOSFET-based half-bridge module in Table 6.3.

Of course, it is challenging to evaluate performance through absolute value comparisons due to differences in rated power, current capacity, and structural form. However, it is important to highlight that the designed module has taken significant measures to reduce parasitic inductance through careful busbar design of the power terminals. Consequently,

when compared to other module designs, the performance is competitive and demonstrates satisfactory results.



(a) (b)



(c)

Figure 6. 6. (a) Schematic view of the test structure (b) Test condition (c) experimental results over the frequency.

Table 6. 2. Comparison of measurement and simulation results.

	Inductance (nH @75kHz)	*Resistance (mΩ @75kHz)*
Ansys Q3D	*13.9*	*33.6*
Measurement	*15.5*	*35.7*

Table 6. 3. Comparison of different power modules extracted inductances from three different half-bridge module .

Inductance	CAS120M12BM2	CAS300M12BM2	SKM350MB120SCH17
Datasheet	15 nH ($L_{STRAY-2,3}$)	14 nH ($L_{STRAY-2,3}$)	15 nH ($L_{STRAY-2,3}$)
Three-fixture Method	15.61 nH ($L_{STRAY-2,3}$)	14. 06 nH ($L_{STRAY-2,3}$)	14.88 nH ($L_{STRAY-2,3}$)

In the case of polymer-based IMS (Insulated Metal Substrate) technology, the thermal conductivity of the dielectric layer may vary depending on the manufacturer. Due to its relatively poor thermal conductivity, it can pose reliability issues. Therefore, A comprehensive set of reliability tests was conducted to preliminarily validate the proposed SiC IMS module technology. These tests included thermal cycling, thermal shock tests, and power cycling. Each type of stress test was accompanied by non-destructive inspection methods: 3D x-ray tomography was used after thermal cycling, acoustic scan microscopy after thermal shock tests, and acquisition of cumulative and differential structure functions during power cycling. The results from these tests provided insights into the module's performance under various stress conditions, highlighting its reliability and identifying areas for potential improvement or optimization [109].

A. Thermal cycling

Using a thermal chamber, 500 cycles were conducted with temperature variations ranging from 25 to 175 °C. The heating ramp-up time was approximately 30 minutes, followed by a cool-down period of about 40 minutes. During these tests, degradation was monitored at several interfaces: 1) between power terminals and substrate, 2) between chips and substrate, 3) between bond-wires and chips, and 4) between the insulation layer and metal substrate. As shown in Figure 6.7, noticeable degradation occurred primarily in the solder layer of the power terminals, where pre-existing voids from the manufacturing process enlarged.

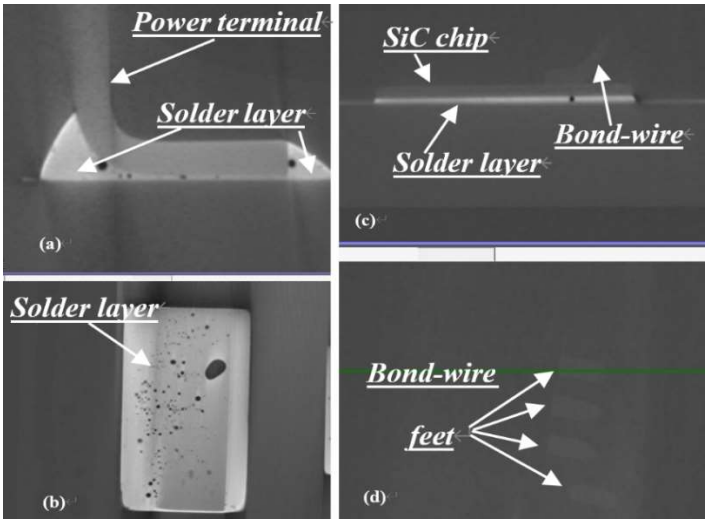
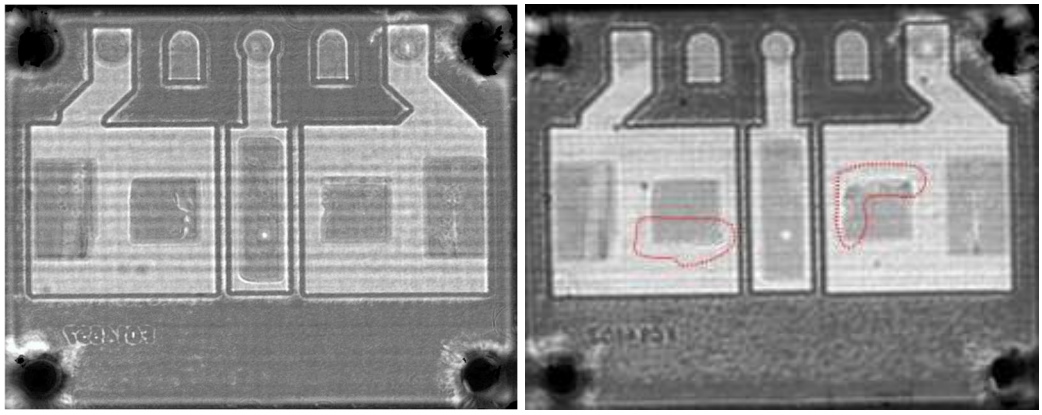


Figure 6. 7. X-ray tomography of BDS after preliminary passive thermal cycling tests.

B. Thermal shock tests

Thermal shock tests were conducted using a dedicated chamber with temperature cycling between -40 and +175 °C. Each temperature level was maintained for 30 minutes. During these tests, issues were observed with the solder interfaces under the chips and power terminals. Figure 6.8 provides a summary of the results, showing signs of solder layer delamination on the sides of both chips.



(a) (b)

Figure 6. 8. Acoustic scan microscopy of interface solder layers between chips and substrate tracks: (a) time-zero state; (b) after 500 cycles.

C. Power cycling

Finally, power cycling tests were conducted using a dedicated test setup that allowed for the acquisition of structure functions. To assess the thermal impedance, the junction temperature of the power semiconductor can be estimated based on the forward diode voltage [110]. In Figure 6.9(a), a measurement circuit has been designed by using a current source with negative gate-source voltages for measuring thermal impedance.

The convection condition has been applied to the natural convection condition. When we applied negative voltages for each gate-source pin, SiC MOSFETs worked as the diode and could conduct the current from source to drain. Moreover, the diode has a forward voltage, which can generate loss. Table 6.4 presents the test condition and measured data. The measured data confirmed the significance of the thermal resistance, which was determined to be 1.563 K/W through a prior thermal analysis simulation in Section 4.2.2.

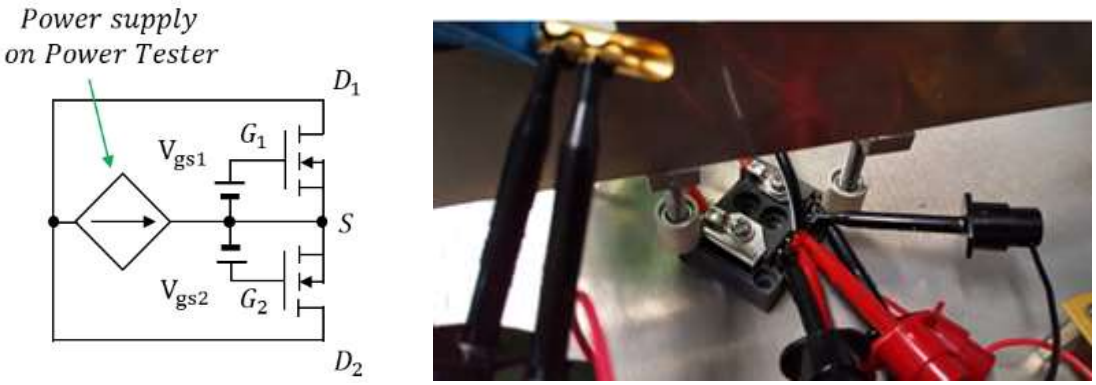


Figure 6. 9. (a) Thermal characterization setup of the bidirectional power switch (b) Test condition.

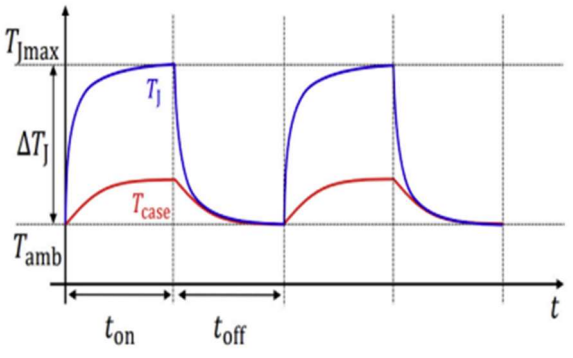
The setup controlled the maximum device temperature excursion (junction temperature, TJ), while also monitoring concurrent changes in the case temperature, TCASE, necessary for the production of structure functions.

Figure 6.10(a) illustrates the test scenario, where ΔT junction-to-case was maintained at 100 K, corresponding to an average power dissipation of about 33 W per chip. Up to 5000

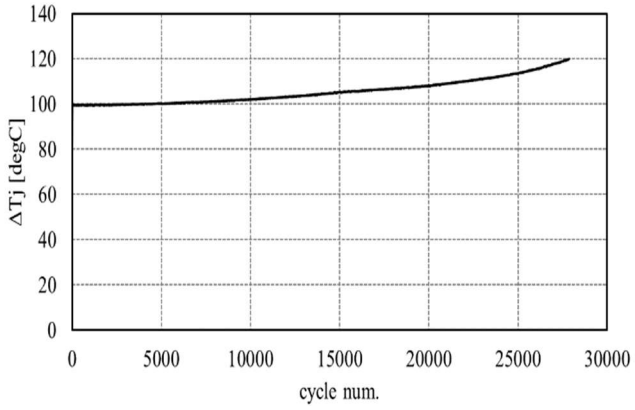
cycles were performed, with structure function data acquired every 1000 cycles. Figure 6.10 (c) presents details of the structure function, showing the top portions of the IMS at time zero and after 3000 cycles. In the differential structure function (k, left vertical axis), the first peak is identified as the interface between the chip and substrate tracks, while the second peak represents the interface between the insulating polymer layer and the Al substrate. These results indicate initial degradation at the insulating layer-substrate interface, likely due to peeling effects. After conducting 27,859 active cycling experiments, a 20% change in thermal resistance was observed. This significant variation was interpreted as an indication of power module lifetime depletion, leading to the decision to terminate the experiments, as seen in Figure 6.10(b).

Table 6. 4. TEST PARAMETERS AND RESULT OF THERMAL IMPEDANCE.

Parameter	*Value*	*Remark*
Gate-Source Voltage	*-9V*	*Vgs1 = Vgs2*
Heating time (t_{on})	*5 sec.*	
Cooling time (t_{off})	*15 sec.*	
Coolant (T_{amb})	*25 ºC*	
Input Current	*16.6 A*	*ΔT_J = 100 ºC*
Drain-Drain Voltage	*3.996 V*	
Total heating power	*66.34 W (33.17 W/chip)*	*ΔT_J = 100 ºC*
Total thermal resistance	*1.507 K/W*	



(a)



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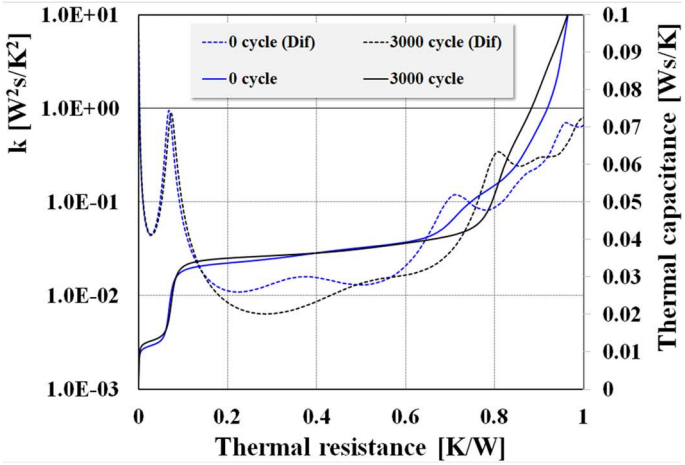


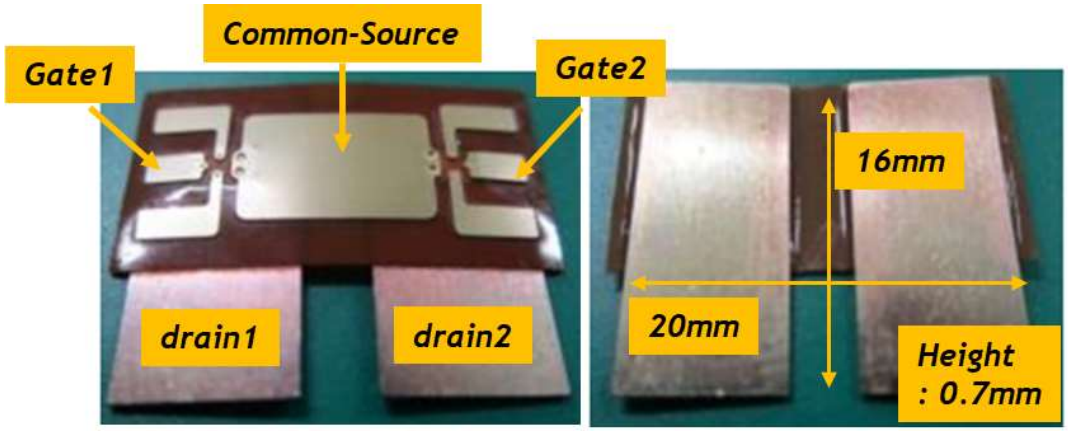
(c)

Figure 6. 10. (a) Power cycle test scenario, (b) Graph of the ΔT_j following the repetition of the active cycling test, (c) Cumulative and differential structure functions

6.2.2 POL-bidirectional switch Prototyping and Validation

Next, the prototype of the bidirectional switch suitable for high-temperature operation, which incorporates Power Overlay (POL) technology, will be examined.

A crucial aspect of developing the POL BDS prototype involves applying underfill gel between the interlayer and the SiC chips. This gel insulates against environmental contaminants and enhances the assembly's ability to withstand voltage. However, the gel flow is hindered by the bending of the interlayer, which is inevitable during the chip-joining process. A high-temperature (225°C) soft silicone gel was employed to mitigate this issue. Figure 6.11 displays one of the 20 prototype switches produced. A specially developed vacuum soaking and curing method achieved effective insulation of all switches, with no visible air bubbles detected upon optical inspection. Subsequently, the samples underwent Ar-plasma cleaning. All fabricated samples were tested for voltage withstand capability and mechanical integrity at a temperature of 200°C over 12 hours.



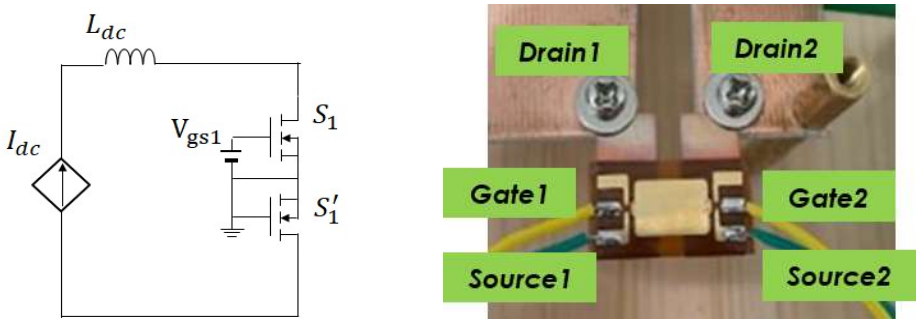
(a) (b)

Figure 6. 11. Prototype of the POL bi-directional module; (a) top view, (b) bottom view.

A. Thermal load test

A circuit resembling the one depicted in Figure 6.12 (a) was constructed to study current conduction at high temperatures. This circuit simulates a typical circulating current

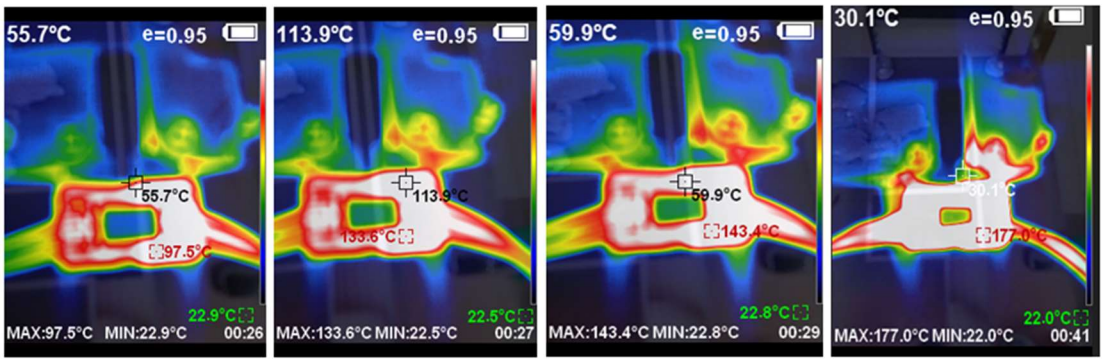
sequence observed in current source inverters, a major application area addressed in this study. The input power source provided constant DC current, stabilized by a DC link inductor of 10mH to minimize current fluctuations. The bidirectional switch was configured to function as a diode tailored to the specific application field.



(a) (b)

Figure 6. 12. Experimental setup for the high-temperature current conduction test. (a) Experimental Circuit (b) Experimental Configuration.

During the experiment, 15 V was applied solely to Gate1 to activate a single switch, while the other switch was freewheeled using its inherent body diode, as depicted in Figure 6.12 (b). A maximum current of 2 A was applied at an ambient temperature of 22 degrees Celsius. Measurements of the voltage between the drain and the drain indicated a power loss of approximately 5 W at around 2.5 V.



(a) (b) (c) (d)

Figure 6. 13. Evaluation of designed power module high temperature electrical experiment with thermal imaging camera.

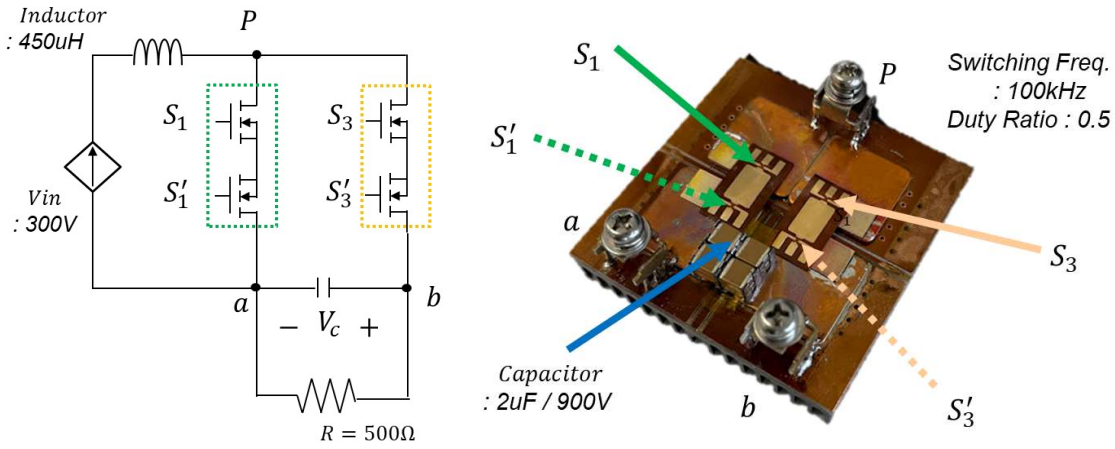
Figure 6.13 presents thermal imaging results captured using a thermal camera to monitor junction temperatures, reaching around 200 degrees Celsius. Sequential images (a) to (d) in Figure 6.13 depict different time intervals, where white regions denote areas near maximum temperature and black regions represent cooler areas. The highest and lowest temperatures recorded in each image are annotated for reference. In Figure 6.13 (a), it is evident that the right SiC MOSFET is turned off, resulting in current flow through its body diode, leading to higher power dissipation compared to the turned-on SiC MOSFET on the left. Consequently, significant heat generation and subsequent dissipation occur in the semiconductor section on the right. Temperature measurements indicated a maximum of approximately 180 degrees Celsius, with a peak temperature of 177 degrees Celsius observed in Figure 6.13 (d). Given the internal temperature was presumed to have reached 200 degrees Celsius, the maximum temperature test was concluded under these conditions [111]. Both maximum temperature and response time are influenced by heat spread design. Before implementing the cooling system, experiments were conducted to assess electrical current behavior at high temperatures without using a heat sink, except for the power conduction connection. One power semiconductor experienced a 5 W power loss, half the simulated value, yet temperatures rapidly exceeded 200 degrees Celsius.

The design of the POL-based power switch for high-temperature operation fundamentally requires a high-performance cooling system. This necessity appears to have caused a significant increase in performance demands. Consequently, a new test bench was set up to conduct switching tests under high-temperature conditions.

B. Active Thermal Test

One of the challenges in evaluating power switches capable of high-temperature operation is the limited availability of Rogowski coils or current sensing methods that can operate accurately at 200°C. This makes it difficult to fully characterize the switch's performance. To address this, a circuit configuration, as shown in Figure 6.14(a), was implemented. This setup is similar to a double pulse test configuration for bidirectional switches. However, to assess high-temperature operational characteristics, a resistive load

was connected to operate similarly to a boost converter. The actual circuit layout is depicted in Figure 6.14(b). The output filter capacitor used is of type X5R, and to increase the rated voltage, four 1μF/450V MLCC capacitors were connected in series-parallel.



(a) (b)

Figure 6. 14. (a) Switching test circuit diagram of the bi-directional switch, (b) Prototype of the test circuit.

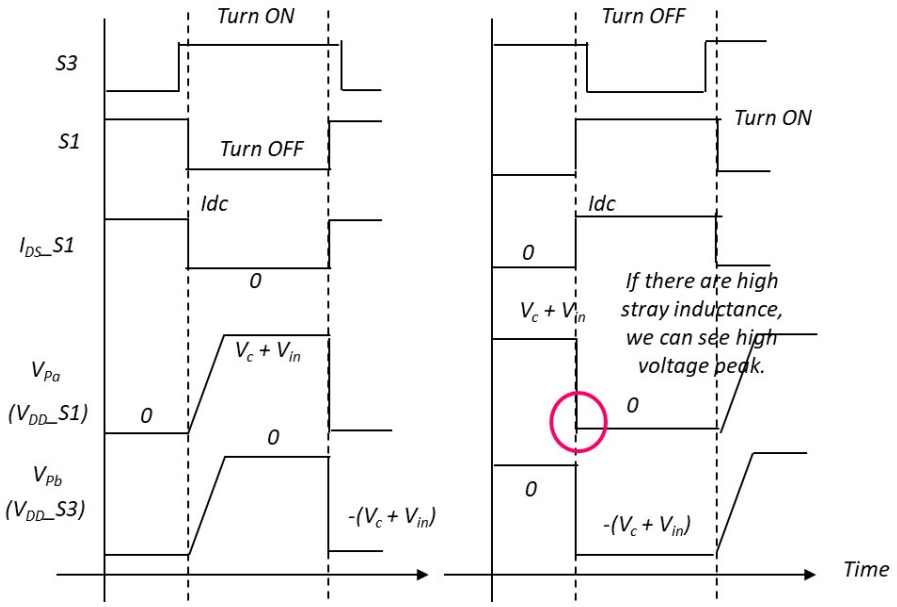


Figure 6. 15. Turn-on and Turn-off behavior of the bi-directional switch with 6.14(a) test circuit.

As shown in Figure 6.15, when switch S3 turns on, the input current is delivered as active current to the load, charging the capacitor and raising the voltage. When S3 turns off, in zero current mode, the input current freewheels, causing the inductor current to rise. The filter capacitor starts discharging to continuously supply energy to the load. Therefore, if there is significant parasitic inductance, voltage ripple can be observed when switch S1 turns on, unaffected by the capacitor. This experimental circuit allows for measuring the input/output power, providing insights into the losses occurring across the entire switch.

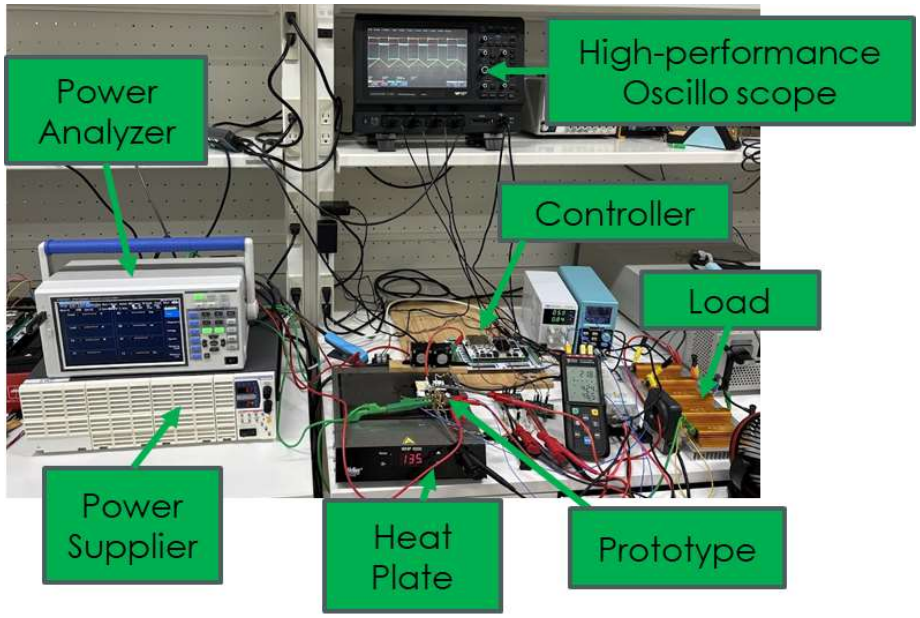


Figure 6. 16. Active thermal test set-up with heat plate.

Figure 6.16 shows the experimental setup used for testing. To simulate the motor windings, a heat plate was used to continuously apply heat, maintaining the temperature at 135 degrees Celsius. The test was conducted after a significant amount of time had passed, allowing the switch's temperature to reach the set point despite heat exchange with the surrounding air. The switching frequency was set to 100 kHz, with an input voltage of 300 V, and an overlap time of 200 ns was applied. Although the duty cycle was fixed at 50%, a slight imbalance was observed due to the overlap time, resulting in a drain-to-drain voltage output of 627 V, which is slightly higher than double the input voltage, as shown in Figure 6.17. A power analyzer measured the input power by detecting the current and

voltage behind the inductor, while the output power was measured by detecting the voltage across the output capacitor and the current flowing to the resistive load.

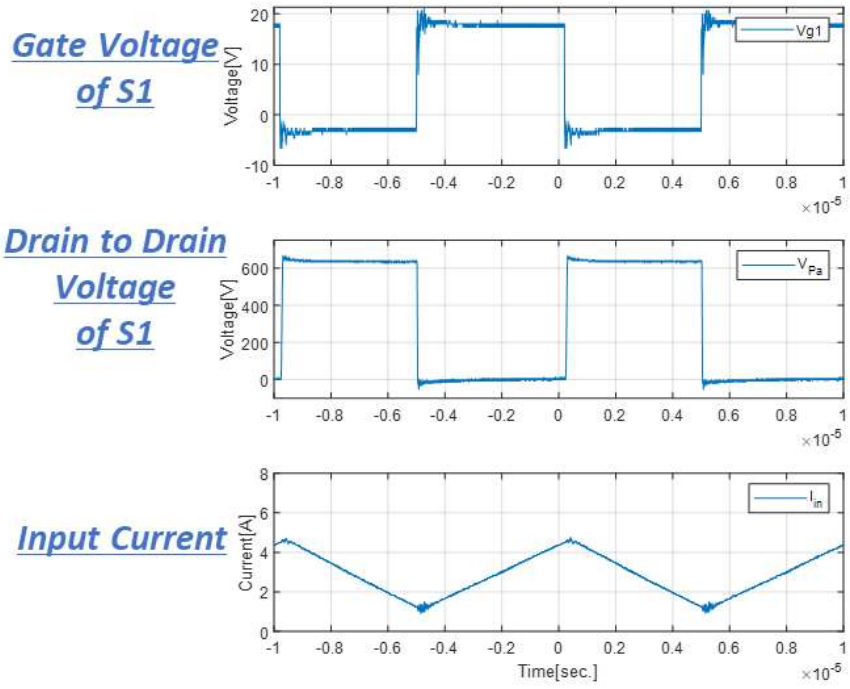


Figure 6. 17. Experimental results with 300Vin at approx..200°C junction temperature

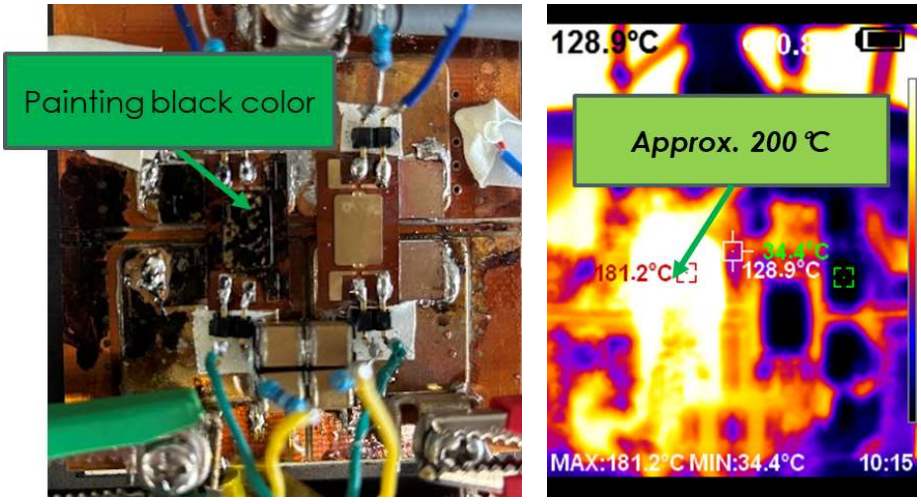


Figure 6. 18. The experimental set-up and the result of the thermal image camera.

Table 6. 5. TEST PARAMETERS AND RESULT.

	Measured Value	Remark
$V_{D-D.S1}$	419.9 Vrms	
V_{cap}	627.4 Vrms	
I_{in}	2.85 Arms	Input current
I_{out}	1.25 Arms	Load current
Pin	807.98 W	
Pout	781.84 W	
Ploss	26.14 W	Per Switch approx.13W
V_{gs}	18V / -4V	

In Figure 6.18, black paint was applied to reduce errors in the temperature measurements taken by the thermal camera. The measured data can be found in Table 6.5. The total measured loss was 26.14W. Assuming that the losses are nearly identical for the two switches, each switch is estimated to have a loss of approximately 13W. The bidirectional switch contains two SiC MOSFET chips. Most losses are expected to occur in the upper switch due to conduction and switching losses, while the lower switch primarily experiences conduction losses due to zero-voltage switching. Consequently, around 10W of losses occur in the upper switch, with an increase from approximately 135°C to around 200°C under 10W loss conditions. This observation aligns closely with the simulation results discussed in Section 4.3.3.

Through this experiment, the high-temperature operational performance was verified with approximately 780W load testing at 200°C and a switching frequency of 100kHz.

6.3 Functional demonstration

Finally, to implement and demonstrate the AC current sensor-less controller, the controller was configured using Imperix, with the unique switching sequences of the PWM implemented through FPGA [112].

6.3.1 AC Current Sensor-less Control

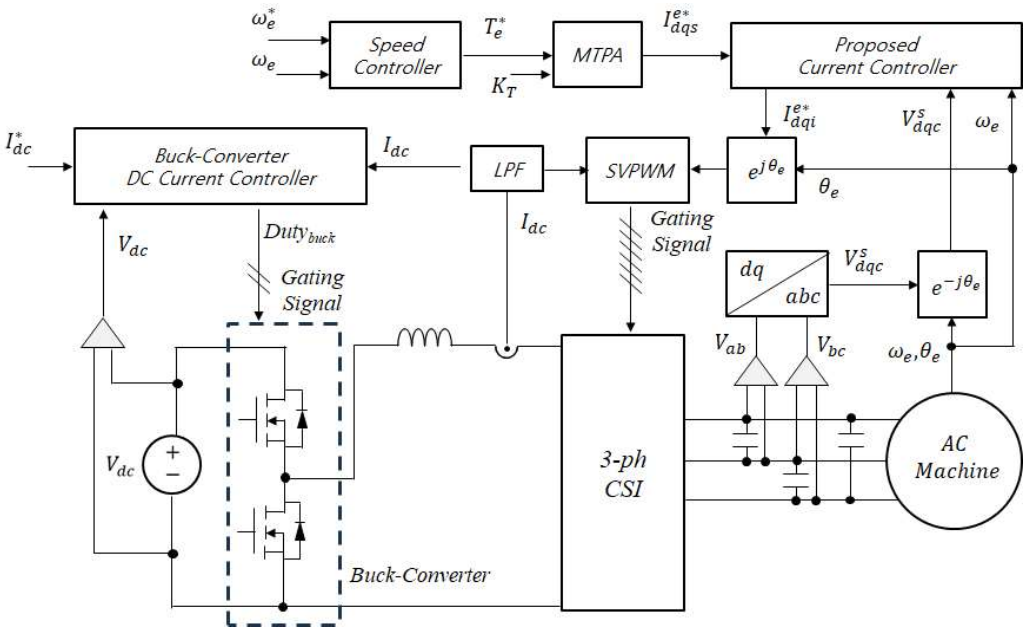


Figure 6. 19. Overall system setup of Buck-CSI-fed AC Motor with AC current sensor-less current controller

In the system configuration illustrated in Figure 6.19, two discrete SiC MOSFETs were used in the DC-DC Buck converter for DC current control. The input voltage was set to 155 Vdc, aligning with the Japanese power supply standard of 110Vac. The output voltage was connected to the center of the top surface of the Printed Circuit Board (PCB) of the Current Source Inverter (CSI) through the DC link inductor, with the ground connected to the bottom center. For DC current control, a single current sensor and one input voltage

sensor were utilized. A Proportional-Integral (PI) controller was implemented for current regulation, as depicted in Figure 6.20.

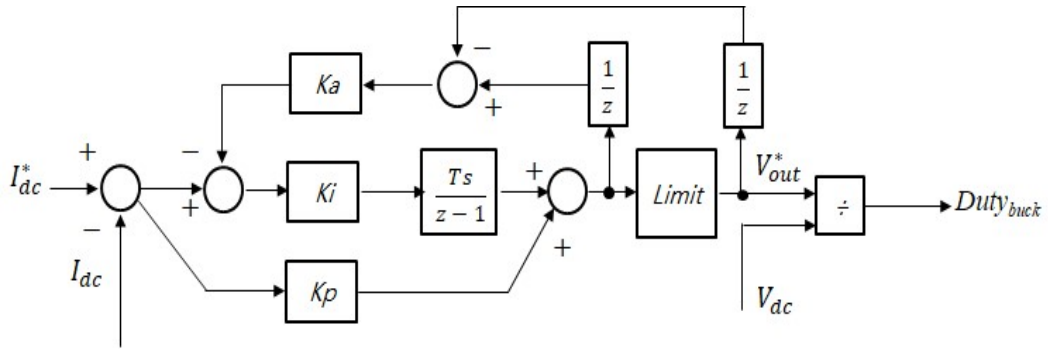
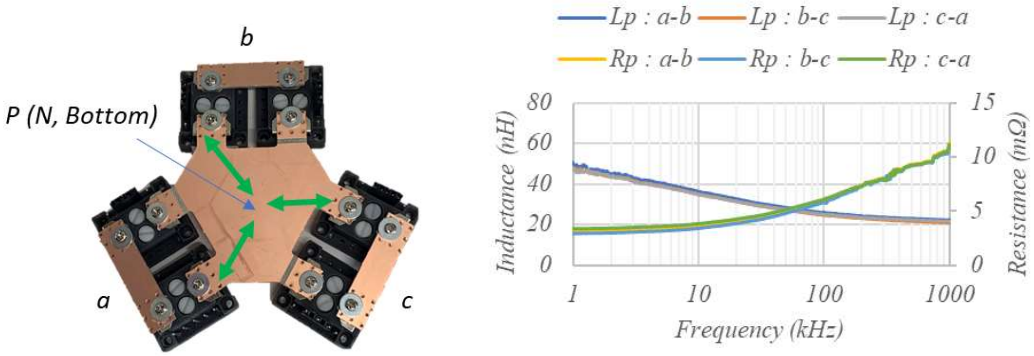


Figure 6. 20. The Structure of the current controller with anti-windup of the Buck Converter

Furthermore, a symmetrical structure was employed in designing the inverter PCB, as shown in Figure 6.21 (a), to mitigate imbalances caused by parasitic inductance during interphase current conduction. Each output, denoted as a, b, and c, is securely connected to the three-phase connection of the motor.



(a) (b)

Figure 6. 21. (a) Based on the designed IMS-based bidirectional switch, symmetrical structure PCB of the three-phase CSI, (b) the measurement result of the line-to-line impedance

The applied current was tested within the range of 2 Arms to adhere to the limitations of the applied motor system under load (Figure 6.23). Detailed motor and control parameters

are provided in Table 6.6. In Figure 6.22, the electrical speed (ω_e), calculated based on the encoder, and ω_e^* representing the target electrical speed, are illustrated. The speed controller employed a standard Integral-Proportional controller. As the applied motor had identical L_d and L_q values, the speed controller's output torque was transformed using motor parameters and used as a current command on the q-axis (the active power axis), with the d-axis current command set to zero.

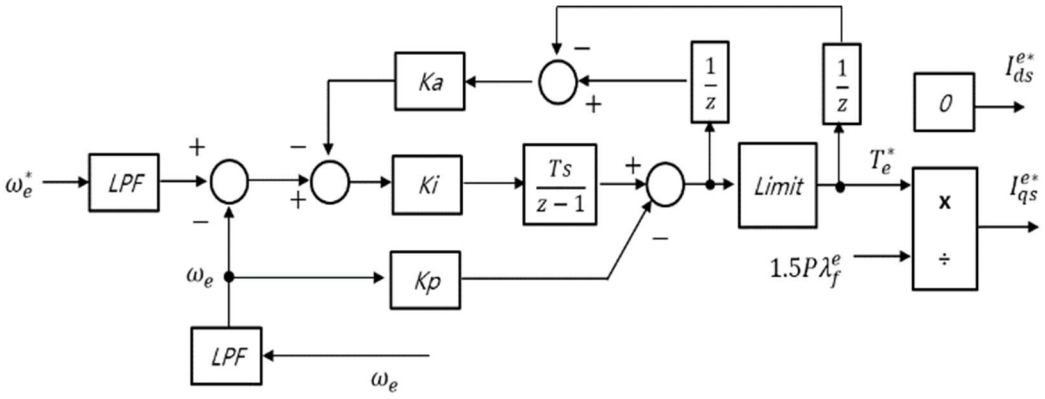


Figure 6. 22. The Structure of the speed controller with IP control

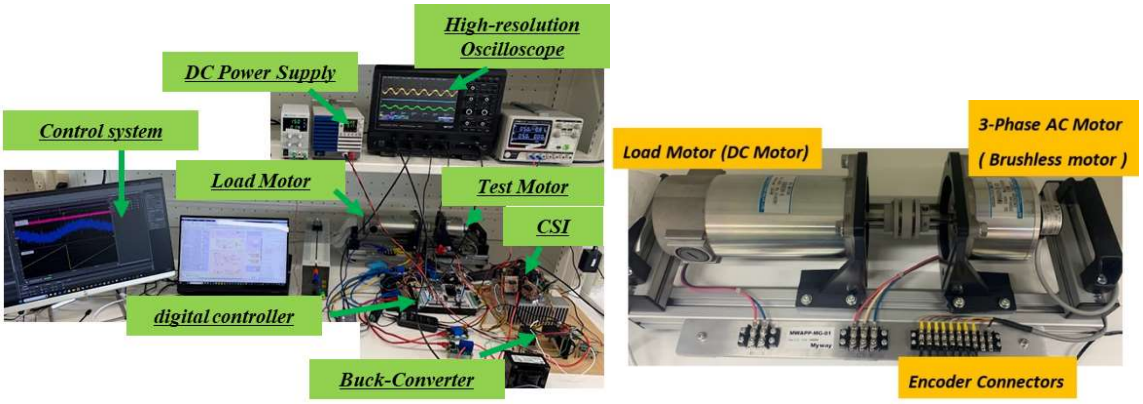


Figure 6. 23. The experimental set-up with motor test bench (RM86A20-2-E8 [113])

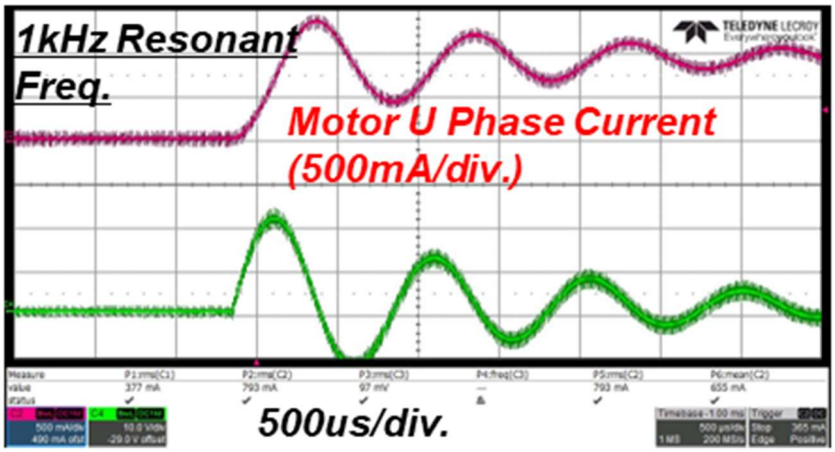
All these motor tests were conducted in the experimental setup depicted in Figure 6.25. The performance of the proposed current controller is illustrated in Figure 6.24. When DC current is applied to the armature, the motor current phase (indicated in red, labeled as the U phase on the motor side) and the motor line-to-line voltage (indicated in green, representing the a-b line-to-line inverter voltage) were monitored. Without the proposed

controller, Figure 6.24 (a) shows oscillations caused by the resonance between the filter capacitor and motor inductance. In contrast, Figure 6.24 (b) demonstrates that the proposed current controller effectively manages the target current by mitigating this resonance.

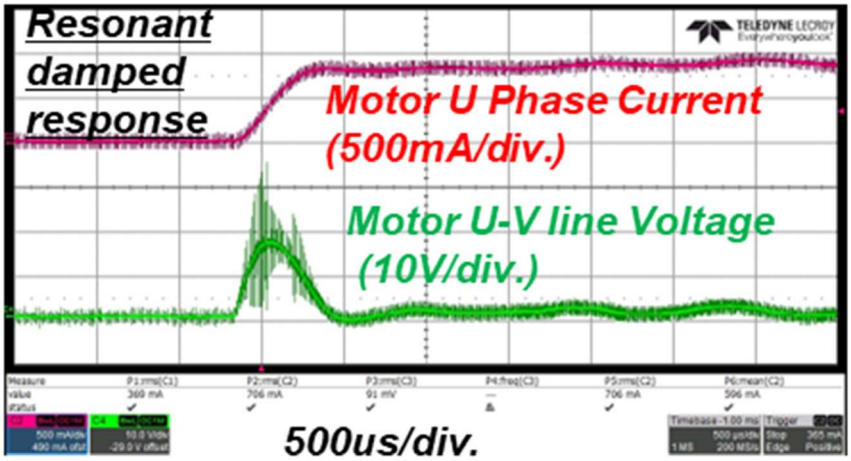
Table 6. 6. MOTOR AND EXPERIMENTAL PARAMETERS.

	Parameter	*Value*	*Remark*
Buck-CSI	Switching Frequency	80kHz	Buck and CSI
	DC Link Capacitor	11.7 uF	3.9uF/800Vdc
	DC current sensor	LA100-P	1 EA
	Voltage sensor	LV25-P	3 EA
	Filter capacitor	3.9 uF	3 EA
	DC inductor	10mH	1 EA
	Input Voltage	150V	Vdc
	DC current reference	3A	Buck Converter
	Overlap time	200ns	
	Dead time	200ns	
	Rv	40	Control Gain
Test Motor [112]	Model Name	RM86A20-2-E8	
	Pole	8	
	Phase inductance	4mH	$Ld = Lq$
	Phase resistance	0.9 ohm	Rs
	Magnetic flux linkage	0.045	λ_f
	Rated current	2A	
	Max. speed	2500 rpm	
	Harmonics EMF	10%	
	Incremental Encoder	1024	pulse per rotation

The motor used in the test has approximately 10% of induced voltage distortion, resulting in the presence of harmonics in the motor current.



(a)



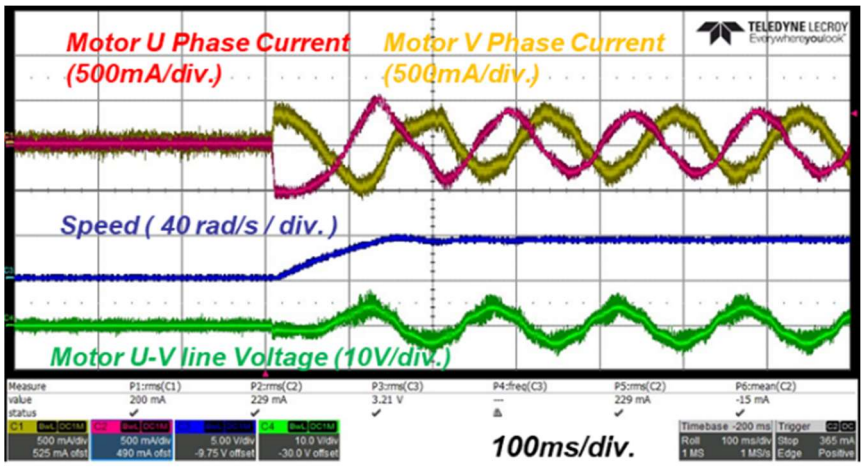
(b)

Figure 6. 24. (a) open-loop response at unit current step input (b) closed-loop response at unit current step input

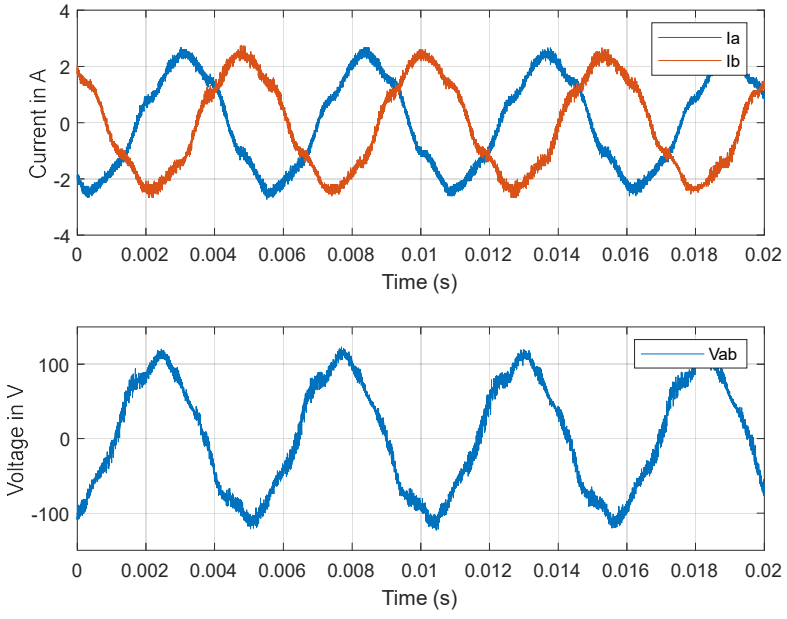
Subsequently, a motor driving test was conducted. Figure 6.25 (a) confirms that the current controller performs adequately, even with rapid changes in current during motor startup. Additionally, the controller was validated at the highest speed of the applied motor, as shown in Figure 6.25 (b).

The study further demonstrated that the absence of output current sensors, coupled with high-frequency sampling in the current source inverter, allows for the creation of a streamlined controller, ensuring effective motor control performance. The experimental results indicate that the custom power switch, designed for high-frequency switching, simplifies the system and introduces an innovative control methodology.

Initially applied in a three-phase motor drive system, this validated design holds promise for opening novel possibilities in Integrated Modular Motor Drive systems. While modular designs with direct coupling to motor wires or slots may require higher temperature operation and increased control complexity, the simplified systems studied in this research, operating without current sensors, are anticipated to find broader applications in future research.



(a)



(b)

Figure 6. 25. (a) Step response with the proposed current control from 0 rpm to 100 rpm. (b) experimental result at 2500 rpm

7. Conclusions and Future Work

In this dissertation, power electronic topologies, power module design, and suitable controller design for implementing structurally and functionally integrated motor drives were investigated. To select the appropriate topology, existing research was compared and analyzed, identifying the current source inverter (CSI) as the optimal choice. A prototype was developed to verify its efficiency.

Additionally, a new integrated power module design based on Power Overlay (POL) technology, suitable for high-temperature operation and high-speed switching, was proposed. The prototype of this module was constructed, and its operation was validated. Furthermore, a novel, simple motor controller that operates without current sensors, leveraging high-speed switching, was introduced, and its performance was verified.

This chapter summarizes these key research achievements and discusses potential future research directions.

7.1 Summary of Results

The main related achievements corresponding to the research objectives are summarized as follows:

- **Design and realization of the three-phase current source inverter with bi-directional switches:**

In Chapter 2, the characteristics of WBG semiconductors were examined, and three topologies capable of utilizing high-speed switching were analyzed: Boost-VSI, Buck-CSI, and Buck-Boost Y-inverter. All three topologies possess the capability to boost output voltage higher than the input voltage. Notably, the Y-Inverter offers a significant advantage over other topologies by allowing only the rated voltage of the power switch related to boosting to increase, enhancing its boosting function. Conversely, the Buck-CSI requires the highest number of power switches (when using bidirectional switches), while the Boost-VSI requires the fewest. However, the Boost-VSI suffers from increased losses due to the output filter and requires the largest number of passive components, resulting in a bulky design. The Buck-CSI, while requiring the most power switches, demands the fewest passive components and has minimal losses from the output filter, promising high efficiency. Therefore, this research focused on integrated drives utilizing the CSI topology.

In Chapter 3, the fundamental operation principles were analyzed, and a simulation model was created to examine the performance of various PWM patterns. Based on this analysis, a prototype circuit of the three-phase CSI was developed in Chapter 6.1. The efficiency of the inverter was measured from 200W to 3kW, achieving over 99% efficiency at 100 kHz switching frequency and up to 98% efficiency at 400 kHz switching frequency with 8A DC input currents.

- **Two different technologies based on customizing bi-directional switches are designed to have a potential with high integration with the motor:**

In Chapter 4.1, a review of fundamental theories on power packaging was conducted to design power switches suitable for integration with motors. Integration with motors requires more flexible placement of power switches. Since motors are generally circular, individual switch designs facilitate this configuration better than traditional three-phase inverter integrated power module designs. Consequently, this research aimed to develop discrete custom bidirectional switches.

In Chapter 4.2, a bidirectional switch based on an insulated metal substrate (IMS) using an aluminum heat spreader and polymer film, was designed to reduce mechanical layers. Compared to the conventional DBC method, this design is significantly lighter and offers substantial cost advantages, sufficient to offset the increased costs of SiC MOSFETs. However, the insulating layer's poor thermal conductivity necessitates thorough thermal analysis and reliability testing. Therefore, in Chapter 6.2.1, a prototype was developed, and three reliability tests were conducted. Through active cycling tests, changes in thermal resistance were observed, and a more than 20% change in thermal resistance was detected after approximately 27,000 cycles of 100-degree temperature variation, indicating the power switch's end of life. Although it is challenging to guarantee superior reliability compared to conventional methods, the design offers sufficient reliability relative to its cost for market consideration. However, operating temperatures above 175 degrees are still limited by bond wires, making their use in integrated motor drivers restrictive.

To address this, an idea based on Power Overlay (POL) technology, which allows for high-temperature operation and significantly reduces parasitic inductance by eliminating bond wires, was proposed in Chapter 4.3. The concept of directly connecting to motor wires without using DBC, thus increasing power density, could provide a competitive solution in applications with robust cooling systems. The design, rated for 3 kW, resulted in a very lightweight module measuring 20x10x0.7mm with a parasitic inductance of 4nH. In Chapter 6.2.2, the design was validated by setting a heat plate to 135 degrees and

observing the switching operation under a single-phase about 800W DC voltage load condition, where the temperature increased to about 200 degrees with a loss of approximately 13W.

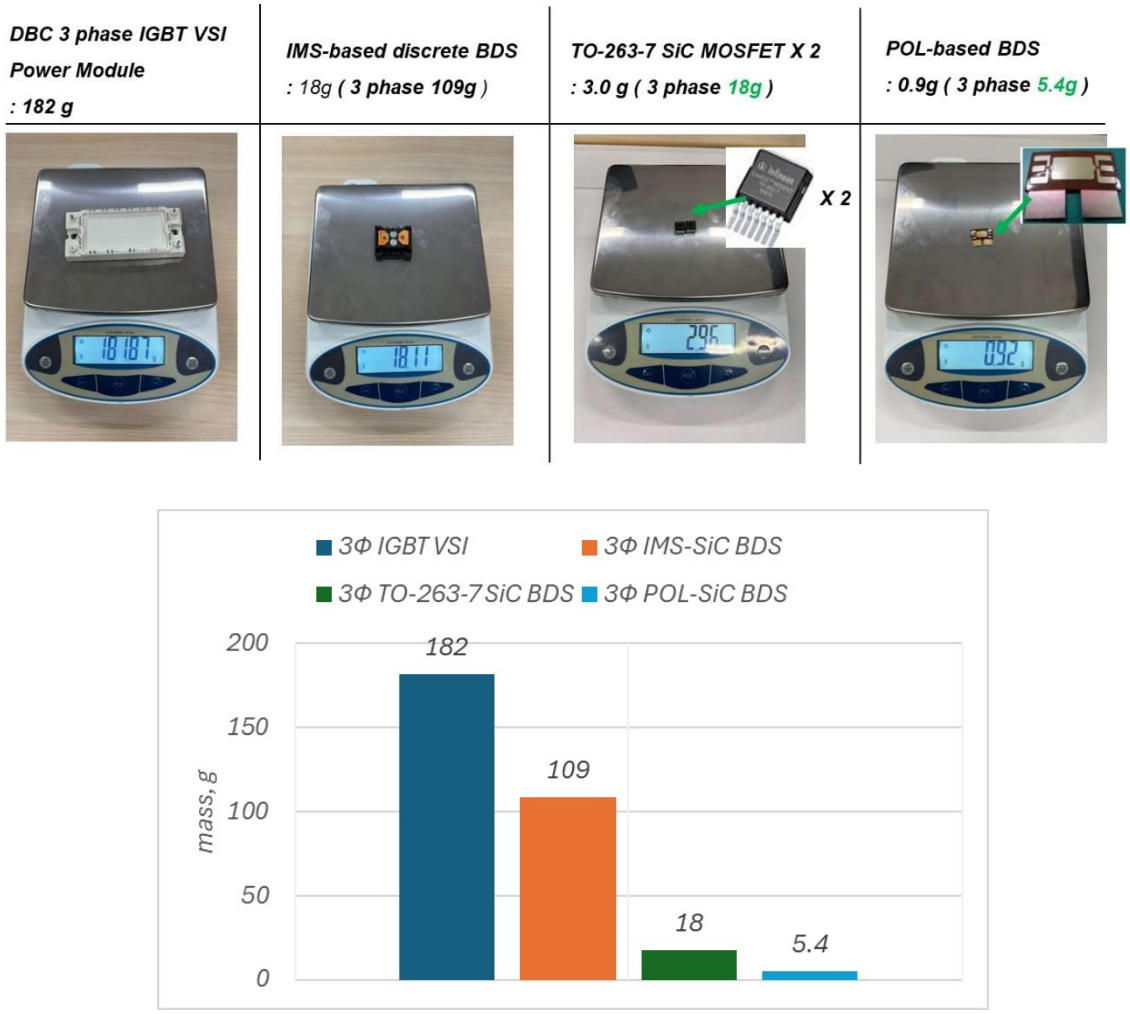


Figure 7. 1 Comparison the mass between typical power module with designed power packaging

Finally, in Figure 7.1, a comparison of the weight of power modules with similar power capacities was made. Although it is challenging to make a fair comparison due to differences in operating temperature and cooling conditions, the designed module's lightweight advantage can be observed when compared to commercially available packages.

- **Proposed AC-current sensor-less current controller designed is validated and demonstrated in the Buck-CSI motor drive.**

In Chapter 5.1, the fundamentals of motor control and the commonly used FOC (Field-Oriented Control) for PMSM current control were examined. Building on this foundation, Chapter 5.2 explored the typical motor controllers for CSI, which have a more complex structure compared to conventional three-phase VSI. Based on this analysis, a simplified motor current controller that does not require current sensors was proposed and designed, utilizing capacitor voltage for current control.

The designed controller was implemented using the Imperix CPU, with PWM overlap time managed by FPGA, as discussed in Chapter 6.3. The controller operated at 80kHz and was validated through DC alignment current control in a fixed coordinate system. Motor load tests confirmed that the designed controller could operate without motor current sensors, even during rotational drive.

This approach simplifies the traditionally complex control structure of CSIs and reduces the number of current sensors, offering a cost advantage. Additionally, the absence of current sensors reduces the overall volume, which is particularly beneficial in integrated motor drives where high ambient temperatures can pose challenges for Hall-type current sensors. This solution holds significant potential for addressing these issues.

7.2 Future Work

The research conducted for the Ph.D. program was carried out as described above. This study encompassed a broad range of topics, including analyzing and designing power electronics topologies, designing and validating power switches, and developing new control strategies utilizing high-speed sampling and controllers like FPGA. The primary objective of this research was to obtain a Ph.D. degree by proposing differentiated ideas and validating and implementing the feasibility of the technology. Typically, such projects require a group or team-based approach with task distribution and personnel from industrial sectors. Therefore, it is firmly believed that further research can deepen the insights explored in this thesis and develop them into practical and effective products.

Firstly, the hardware design suitable for an integrated motor drive is required. This research did not address the mechanical challenges necessary for the actual integration with motor windings. Therefore, the power electronics topology and power modules were tested and verified separately. A mechanical approach is needed to determine how to design or integrate motor windings. Consequently, the appropriate power electronics circuit design must also be considered.

Secondly, reliability test results for the POL technology integrated with the motor structure are required. Currently, the absence of an enclosure means that the system is susceptible to environmental factors such as dust. Feedback from manufacturers suggested refraining from reliability testing under these conditions. After discussing and finalizing the integrated motor structure, conducting reliability tests will provide a more comprehensive technical understanding.

Thirdly, the controller validation needs to be extended to various motors. This research was only validated on a single motor test bench. Evaluating and analyzing the controller on different motors could reveal technical limitations and breakthrough ideas.

With growing interest in these research, it is hoped that extensive discussions and further research will lead to technological advancements.

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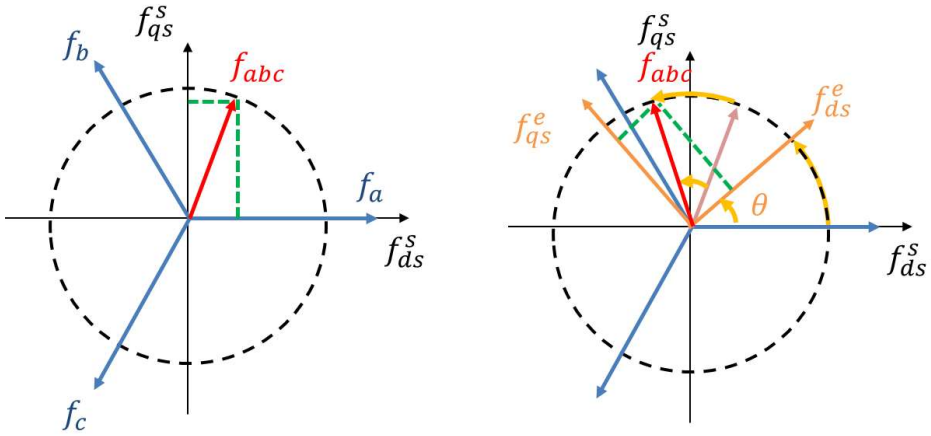
Appendix.

Appendix. A: Reference Frame theory

For AC motors (such as induction motors and synchronous motors), the inductance is a function of the motor's position, resulting in time-varying differential equations. Reference frame theory is used to simplify the analysis of these time-varying differential equations.

In three-phase motors, the variables (such as voltages and currents) in the a, b, c phases are typically time-varying and can be complex to analyze directly. By transforming these variables into the d, q, n coordinate system, we convert the time-varying AC quantities into DC quantities in the rotor reference frame, which simplifies the analysis and control of the motor.



(a) (b)

Figure A.1 (a) stationary reference frame (b) synchronous reference frame.

Here, θ (theta) is the transformation angle of the coordinate system between the a-phase of the stator and the d-axis of the rotating reference frame. It is measured counterclockwise from the a-phase to the d-axis.

$$\theta = \int_0^t \omega(\tau)\, d\tau + \theta(0) \tag{A.1}$$

$\theta(0)$ represents the initial position of the d-axis relative to the a-phase when the system starts and usually set to 0 for simplicity. ω is the angular velocity of the rotating coordinates system.

Figure A.1 (a) shows the stationary reference frame when the angular velocity (ω) is zero. The reference frame is fixed relative to the stator and does not rotate. It is useful for the stator variable directly. In this frame, AC variables appear as time-varying sinusoidal quantities.

$$\mathbf{f}_{\boldsymbol{dqs}}^{\boldsymbol{s}} = \frac{2}{3}(f_a + \mathbf{a} f_b + \mathbf{a}^2 f_c),\ \mathbf{a} = e^{j\frac{2\pi}{3}} \tag{A.2}$$

$$\begin{bmatrix} f_{ds}^s \\ f_{qs}^s \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{A.3}$$

$$f_a = \mathrm{Re}\left(\mathbf{f}_{\boldsymbol{dqs}}^{\boldsymbol{s}}\right), f_b = \mathrm{Re}\left(\mathbf{a^2 f}_{\boldsymbol{dqs}}^{\boldsymbol{s}}\right), f_c = \mathrm{Re}\left(\mathbf{a f}_{\boldsymbol{dqs}}^{\boldsymbol{s}}\right) \tag{A.4}$$

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} f_{ds}^s \\ f_{qs}^s \end{bmatrix} \tag{A.5}$$

In general, such coordinate transformations can be expressed using complex vectors or matrices. Eq. (A.2) shows the transformation of a three-phase coordinate system into a stationary coordinate system using complex vectors. Eq. (A.3) provides a matrix representation that is easy to implement in a program. The inverse transformations are shown in Eq. (A.4) and (A.5).

If the ω is the same as the electrical angular speed (ω_e), we call it the synchronous reference frame. In this frame, the coordinate system rotates at the same speed as the rotating magnetic field of the stator. Also, the d-axis aligns with the rotor's magnetic field

in a synchronous machine. It is used to simplify the analysis of synchronous machines, where the electrical variable appears as DC values when viewed from this frame. If this is expressed in the following Eq. (A.6) and (A.7) as a complex vector and matrix, respectively, the inverse transformation can be seen in Eq. (A.8) and (A.9).

$$\mathbf{f}^{\boldsymbol{e}}_{\boldsymbol{dqs}} = \mathbf{f}^{\boldsymbol{s}}_{\boldsymbol{dqs}} e^{-j\theta} \tag{A.6}$$

$$\begin{bmatrix} f^e_{ds} \\ f^e_{qs} \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} f^s_{ds} \\ f^s_{qs} \end{bmatrix} \tag{A.7}$$

$$\mathbf{f}^{\boldsymbol{s}}_{\boldsymbol{dqs}} = \mathbf{f}^{\boldsymbol{e}}_{\boldsymbol{dqs}} e^{j\theta} \tag{A.8}$$

$$\begin{bmatrix} f^s_{ds} \\ f^s_{qs} \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} f^e_{ds} \\ f^e_{qs} \end{bmatrix} \tag{A.9}$$

Based on these formulas, three-phase AC voltage, current, magnetic flux, etc., can be expressed as two AC signals through the stationary reference frame. These can then be converted into synchronous coordinates with DC signals depending on the speed and position of the synchronized rotor. This can be confirmed through a simple example in Figure A.2.

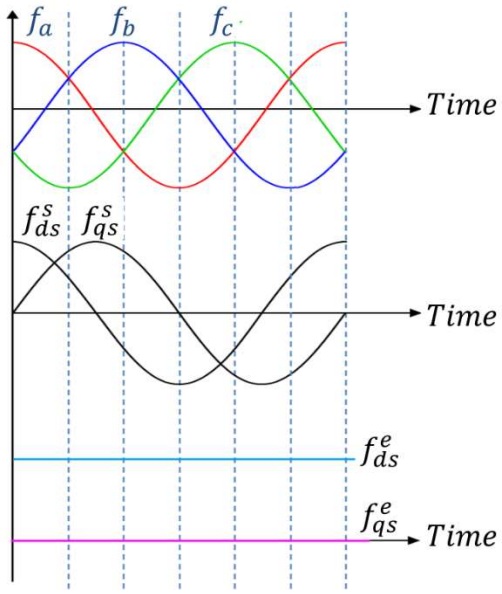


Figure A.2 Example of the reference frame converting; abc reference frame → stationary reference frame → synchronous reference frame.

Appendix. B: Anti-Windup

Physical inputs and outputs in control systems are constrained by physical limits, characterized by upper and lower bounds (Upper Limit and Lower Limit). If only the controller's output is limited, the integrator continues to accumulate its integral value beyond the bounds set for the controller. This issue is termed as wind-up.

Wind-up happens when the integrator accumulates excessively because the controller's output is constrained, irrespective of the physical limits of the system. Even if the error signal changes direction, the integrator retains its accumulated value, leading to incorrect or sluggish responses from the controller to input changes.

Therefore, wind-up occurs due to the integrator's inability to adjust its accumulation rate appropriately when the controller's output is restricted, thus affecting the controller's performance and response time negatively. To mitigate this, anti-windup mechanisms are employed to manage integrator saturation and maintain effective control within specified operational limits.

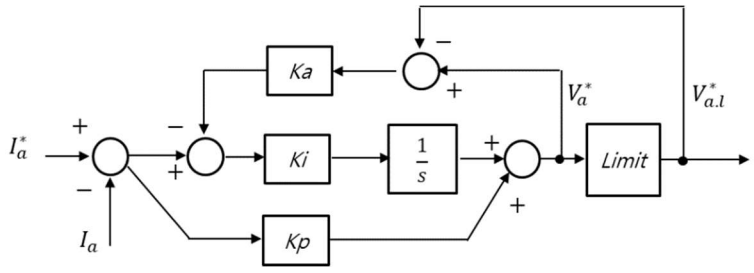


Figure B.1 The PI controller with anti-windup for the current control at RL load.

Figure B.1 illustrates a basic current PI controller with anti-windup for an inductor-resistor ($L_a - R_a$) load. K_p represents the proportional controller gain, while K_i represents the integral controller gain. To implement physical constraints, the limit on the previous stage's voltage command is denoted as V_a^*, and the voltage command after passing through

the limiter is represented as $V_{a.l}^{*}$. The closed-loop transfer function can be summarized by the following equation.

$$I_a(s) = \frac{\frac{K_p}{L_a}s + \frac{K_i}{L_a}}{s^2 + \frac{K_p + R_a}{L_a}s + \frac{K_i}{L_a}} \left[I_a^*(s) - \frac{s + K_a K_i}{K_p s + K_i} \{ V_{a.l}^*(s) - V_a^*(s) \} \right] \qquad (B.1)$$

If the anti-windup gain is defined as $K_a = 1/K_p$, we can derive the transfer function as follows:

$$I_a(s) = \frac{\frac{K_p}{L_a}s + \frac{K_i}{L_a}}{s^2 + \frac{K_p + R_a}{L_a}s + \frac{K_i}{L_a}} \left[I_a^*(s) - \frac{1}{K_p} \{ V_{a.l}^*(s) - V_a^*(s) \} \right] \qquad (B.2)$$

Therefore, by implementing the anti-windup function, the controller ensures that the current command, influenced by the voltage output, remains within specified limits. This design approach effectively reduces integral error accumulation and ensures stable and precise control of the system under varying operational conditions. Such a limiter mechanism plays a crucial role in preventing integrator wind-up and maintaining optimal performance of the control system.

Appendix. C: Review of the Control Theory [101]

In control system design, it's essential to assess how closely a test design aligns with intended outcomes. This is achieved by examining system behavior equations using linear analysis or numerical simulation methods.

Linear dynamic systems are described by differential equations, which can be converted into state-variable form:

$$\dot{\boldsymbol{x}} = \boldsymbol{F}\boldsymbol{x} + \boldsymbol{G}\boldsymbol{u} \tag{C.1}$$

$$\boldsymbol{y} = \boldsymbol{H}\boldsymbol{x} + \boldsymbol{J}\boldsymbol{u} \tag{C.2}$$

Here, x is the state vector, u is the input vector, y is the output vector, F is the system matrix, G is the input matrix, H is the output matrix, and J is a direct transmission matrix.

Using this system description, we see that the second-order differential equation

$$\ddot{\boldsymbol{y}} + 2\zeta\omega_0\dot{y} + \omega_0^2 y = K_o u, \tag{C.3}$$

can be written in the state-variable form as

$$\begin{bmatrix}\dot{x_1}\\ \dot{x_2}\end{bmatrix} = \begin{bmatrix}0 & 1\\ -\omega_0^2 & -2\zeta\omega_0\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}0\\ K_o\end{bmatrix}u \tag{C.4}$$

$$y = \begin{bmatrix}1 & 0\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} \tag{C.5}$$

where the state

$$\boldsymbol{x} = \begin{bmatrix}x_1\\ x_2\end{bmatrix} = \begin{bmatrix}y\\ \dot{y}\end{bmatrix} \tag{C.6}$$

is the vector of variables necessary to describe the system's future behavior, given the initial conditions of those variables.

The Laplace transform is useful for analyzing linear systems with zero initial conditions, converting signal derivatives into algebraic equations.

$$L\{\dot{f}(t)\} = sF(s). \quad (C.7)$$

For the differential equation (C.3), the transfer function G(s) is

$$(s^2 + 2\zeta\omega_0 s + \omega_0^2)Y(s) = K_o U(s), \quad (C.8)$$

$$G(s) = \frac{Y(s)}{U(s)} = \frac{K_o}{s^2 + 2\zeta\omega_0 s + \omega_0^2}. \quad (C.9)$$

The transfer function can be expressed in polynomial form:

$$G(s) = \frac{b_1 s^m + b_2 s^{m-1} + \cdots + b_{m+1}}{a_1 s^n + a_2 s^{n-1} + \cdots + a_{n+1}}. \quad (C.10)$$

Or in zero-pole-gain form:

$$G(s) = \frac{Y(s)}{U(s)} = K\frac{\prod_{i=1}^{m}(s - z_i)}{\prod_{i=1}^{n}(s - p_i)}. \quad (C.11)$$

The poles of G(s) are values of s where G(s) is infinity, and the zeros are where G(s) is zero. For first-order pole:

$$G(s) = \frac{Y(s)}{U(s)} = \frac{1}{s + \sigma}, \quad (C.12)$$

The impulse response is

$$g(t) = e^{-\sigma t}1(t). \quad (C.13)$$

When $\sigma > 0$, the pole is located at When $s < 0$, the exponential decay and the system is said to be stable. Likewise, if $\sigma < 0$, the pole is to the right of the origin; the exponential grows with time and is referred to as unstable.

Stability is determined by the sign of σ. Complex poles are given by

$$s = -\sigma \pm j\omega_d. \quad (C.14)$$

And the corresponding transfer function for a complex pole pair is:

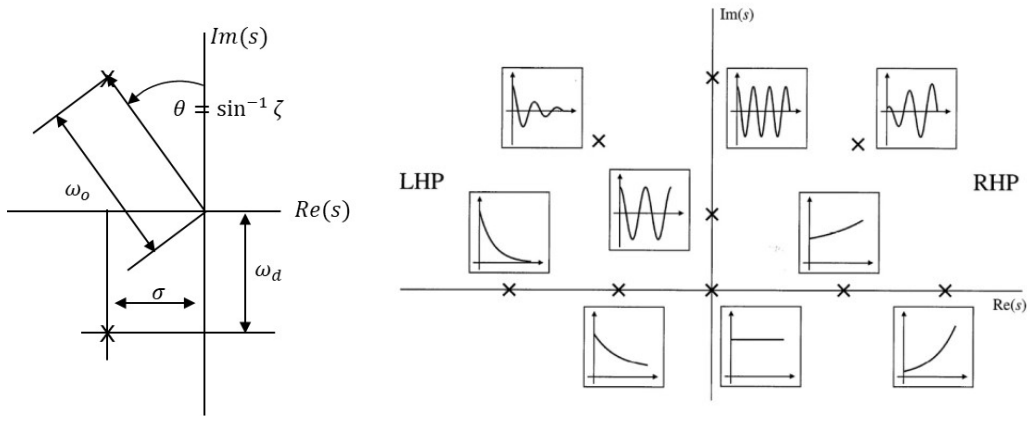
$$U(s) = (s + \sigma - j\omega_d)(s + \sigma + j\omega_d) = (s + \sigma)^2 + \omega_d^2. \quad (C.15)$$

From the expanded form of (C.15), we can identify the damping ratio ζ and undamped natural frequency ω_o.

$$\sigma = \zeta\omega_o \quad and \quad \omega_d = \omega_o\sqrt{1 - \zeta^2}. \tag{C.16}$$

The transfer function for a second-order system with these parameters.

$$G_p(s) = \frac{\omega_n^2}{(s + \zeta\omega_n)^2 + \omega_n^2(1 - \zeta^2)}. \tag{C.17}$$



(a) (b)

Figure C. 1. (a) s-plane plot for a pair of complex poles (b) the relationship between pole locations in the complex s-plane and the corresponding time-domain responses of a system [101].

As shown in Figure C.1, the position of the poles is influenced by the damping factor and the natural frequency. This variation in pole location results in different time-domain responses, such as oscillatory or damped responses, as depicted in Figure C.1(b). Consequently, the design of the pole locations must be tailored to the control system's objectives to achieve the desired response characteristics.

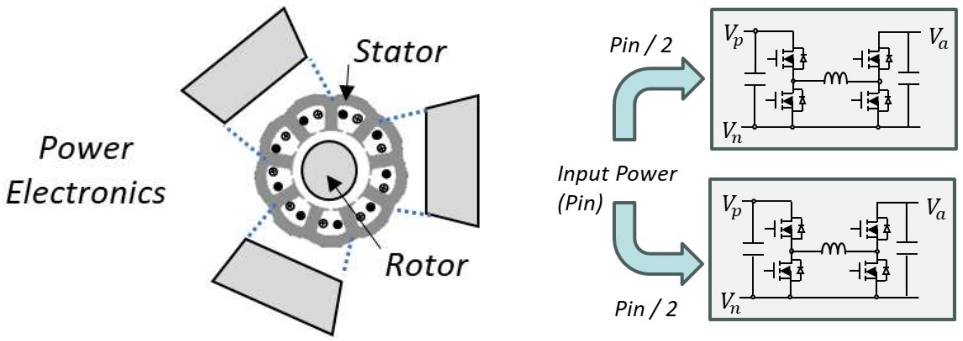
Appendix. D: Optimized control design for the Si-SiC Hybrid interleaved Buck-Boost Y-Inverter with Halbach motor

In this Appendix, we discuss the design of a controller for a Buck-Boost Y-Inverter, leveraging the advantages of a modular design with WBG power switches. Modular design, using identical power electronic circuits, increases rated power and is vital for battery applications where current must increase without raising voltage. High-current systems often adopt modular designs due to the capacity of power switches and passive components.

The Y-Inverter's robust boosting capability allows motor voltage to exceed input voltage, essentially functioning as a four-switch non-isolation buck-boost DC/DC converter. These converters typically use parallel structures to enhance power and enable interleaved driving, reducing ripple currents in passive components. This methodology applies to the Y-Inverter, optimizing passive components in various applications.

However, parallel modular design complicates the controller due to the need for more sensors. Additionally, if one module fails, the system can continue with other modules, though this may cause delays due to imbalances in components and switching cycles. In this study, we designed and validated an optimized controller for a modular Y-Inverter.

D.1. System Description



(a) (b)

Figure D. 1. Modular design for the motor drive (a) Integrated Modular Motor Drive, (b) Two Phase Modulated Y-inverter.

Figure D.1(a) shows an example of the Integrated Modular Motor Drive (IMMD) explained in Chapter 1. This demonstrates how power electronic circuits can be combined in a modular form. The Y-Inverter is well-suited for this modular design. Figure D.1(b) shows that it allows for easy power distribution using identical power electronic circuits. Therefore, this study will explore a modular design using a Y-inverter and develop a suitable controller for it.

D.1.1. Low Voltage based light EV Car

These modular designs are highly suitable for battery-powered electric vehicles. Traditionally, the development of traction drives for hybrid and fully electric vehicles (EVs) has focused on increasing primary source voltage levels, reaching up to 800 V for power ratings over 100 kW. Such high voltages make it possible to create traction drive systems that rely solely on an inverter to power the machine, eliminating the need for voltage step-up DC-DC converters on the input side.

However, a new trend is emerging, characterized by a reduction in power and voltage ratings. Future development is expected to focus more on optimizing the motor's volume and weight by increasing the number of poles in the machine design. This approach raises the required fundamental frequency and amplitude of the supply voltage, starting from a lower input battery voltage.

There is also growing interest in adopting wide-band-gap (WBG) semiconductors, which enable high switching frequencies and efficiencies even at higher voltage ratings. To offset the higher initial cost of this technology, efforts are being made to achieve benefits and savings in other parts of the system through WBG-specific designs. One promising solution gaining widespread interest in this context is the Y-inverter, as discussed in Chapter 2.2.3.

In this work, a motor drive with a nominal rating of 7.5 kW is considered to be supplied by a primary battery with a 60 V nominal rating (48 V min; 72 V max). The specification is derived from an actual commercial light electric vehicle. To demonstrate significant

improvements in overall power density, the single-rotor Halbach machine was custom-designed with a high number of poles and minimum inductances, requiring fundamental electrical frequencies up to about 2 kHz, with phase-to-neutral voltage amplitudes up to 120V.

In the following sections, we will first describe the design of all components of the motor-drive system in detail and then introduce the development and characterization of hardware prototypes.

D.1.2. Halbach Motor with Optimized PM array

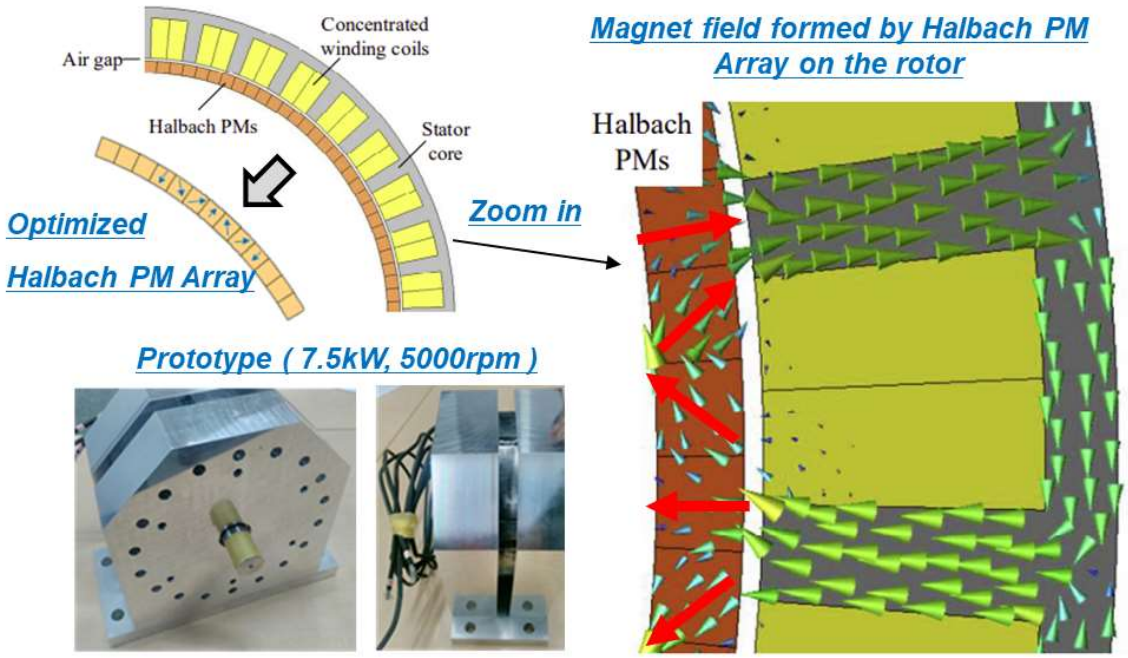


Figure D. 2. Machine design: optimization of Halbach arrays orientation and placement with machine structural features.

Figure D.2 illustrates the single-rotor Halbach EV motor's basic structure, magnetic flux, and optimum magnet placement. The main configuration parameters and coefficients of interest are listed in Table D.1. Several design optimization iterations are carried out to improve the output quality:

- Iron core structure: Iron losses are one of the main components in electric machines. They include two sub-components: hysteresis loss and eddy current loss. Both components typically increase drastically with rotational speed. If crossing of the iron core by the magnetic flux lines can be, as illustrated more in detail in right side of the Fig. D.2, motor efficiency can be significantly improved, especially in the high-speed region.
- High pole-number: This motor adopts a high pole topology (stator/rotor - 36/40) to produce a high and smooth torque within a limited cross-sectional area. However, the high-pole topology inevitably results in a high fundamental frequency of the magnetic flux inside the machine.
- Halbach permanent-magnets magnetic angle: The distribution of flux in the air gap determines the transient torque output of the motor. Results of FE analysis show that the magnetic orientation of the Halbach PM array has a significant impact, for instance, on the torque ripple. After extensively benchmarking design options, the 60° magnetization illustrated in Figure D.2 was chosen as the optimum configuration.

Table D. 1. Torque-Speed and Electrical Characteristics of the Machine

Torque $[N-m]$	**Motor Terminal Current** $[I_{out}, A_{rms}]$	**Motor Phase Voltage** $[V_{out}\, V_{rms}]$	**Speed** $[rpm]$
63.5	106	24	825
50	83	30	1048
40	67	37	1310
30	50	50	1747
20	33	75	2621
12.5	21	120	4193

Additional design considerations aim to contain current density in the windings to reduce copper losses and maximize the motor's lightweight character. The machine was ultimately laid out as a six series x two parallel windings configuration for each phase. With the adopted design choices, the predicted efficiency is $\eta = 93\%$, and the power

density is $PDM = 5.21\ kW/Kg$. Table D.1 summarizes the torque-speed characteristics for the nominal 7.5 kW rating, which also reports the corresponding RMS values of phase-to-neutral voltage and phase current used to inform the Y-Inverter design.

D.1.3. Si-SiC Hybrid Interleaved Y-Inverter

The Y-Inverter, Figure D.3, consists of the output-side Y-interconnection of three dc-dc converter cells, modulated with a sinusoidally varying duty-cycle: the output of each cell is an offset sinusoidal waveform, that is, with non-zero average value, whose minimum and maximum values, relative to the input voltage, depending on the choice of the converter.

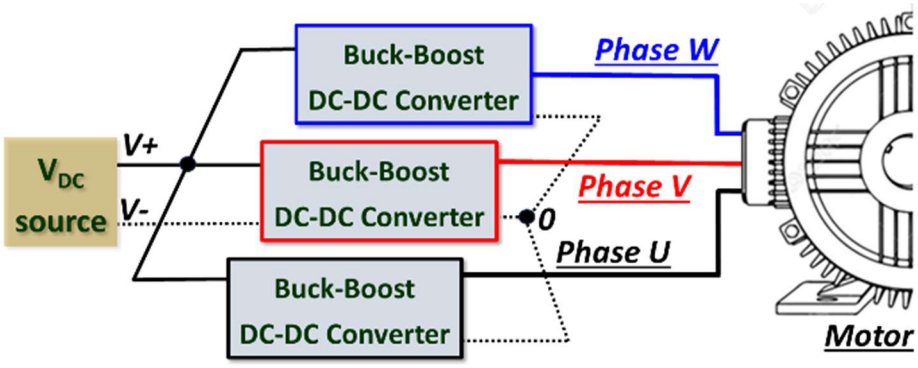


Figure D. 3. Illustration of the Y-Inverter design concept.

If a buck-boost topology is used, then the minimum can be as low as zero and the maximum as high as the converter's boost capability allows. In the three-phase implementation, the offset is canceled out in between phases, yielding sinusoidal phase voltages and currents.

Given the ratings detailed in the previous section, the input side transistors can be rated for relatively low voltage (e.g., 100 V). So, either silicon (Si) MOSFETs or gallium nitride (GaN) HEMTs could be chosen. Here, the choice fell on Si to contain cost. As confirmed in Table 4.1, the maximum voltage for the motor is within 120V, while the output capacitor requires a voltage of approximately 350V or higher. This also affects the rated voltage of

the power switches. On the output side, 650 V-rated devices are ideal for considering both GaN HEMTs and silicon carbide (SiC) MOSFETs. Here, SiC MOSFETs were chosen by virtue of their greater maturity and availability from multiple manufacturers.

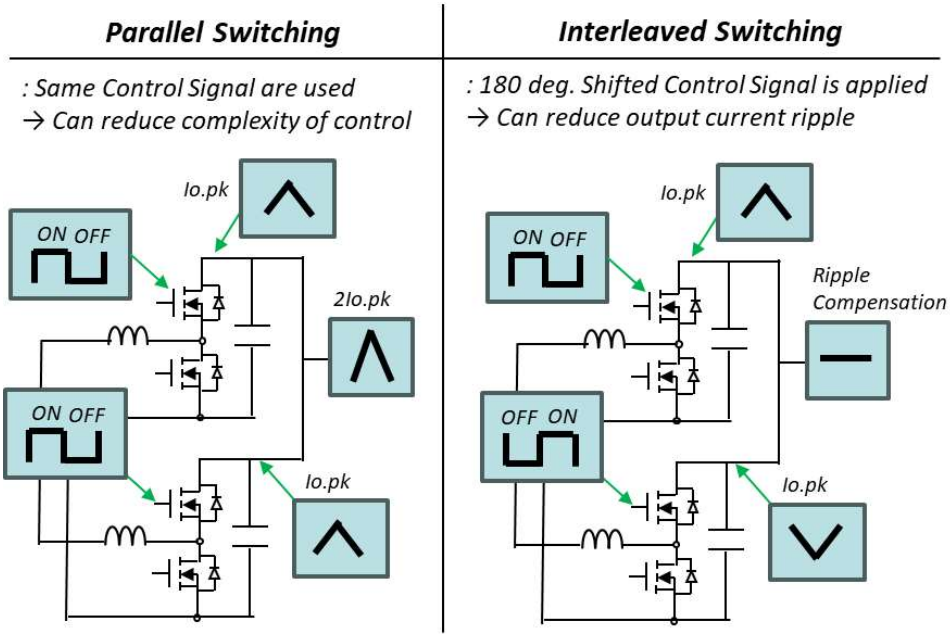


Figure D. 4. The power switch control methodologies for the Two-Interleaved phase Buck-Boost Converter.

To meet the overall rating requirement, more than one switch on the output is required. With a nominal input voltage of 60V, an input current exceeding 125A is required under rated power conditions. Additionally, the increase in the inductor's ripple under boost conditions significantly raises the power switches' current stress.

Therefore, rather than paralleling multiple devices, it opted for an interleaved implementation of a single cell to reduce the size and electro-thermal stress of the passive components, as shown in Figure D.4. The two parallel interleaved switches are operated based on carrier frequencies with a 180-degree phase shift. By shifting the switching signals by 180 degrees, the turn-on timing of the parallel-connected switches is staggered. This alternating turn-on and turn-off over short intervals results in the cancellation of the current ripple in the output capacitor, thereby reducing the output voltage ripple. Consequently, this allows for a reduction in the size of the passive components. Practically,

the Y-inverter's Boost Stage, with its higher current ripple than the Buck's leg, can benefit from the strategic application of SiC MOSFET to reduce ripple.

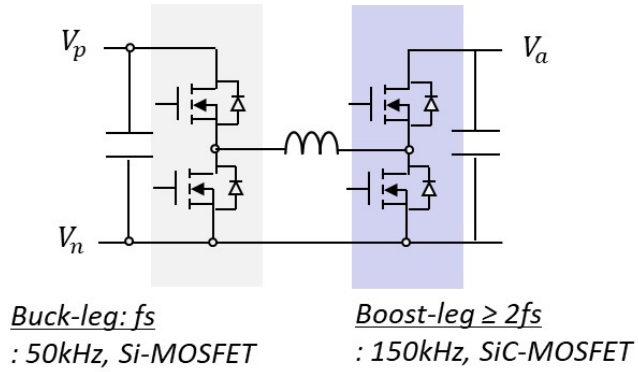


Figure D. 5. Si-SiC Hybrid Configuration in Y-inverter

In summary, the switches in the buck-leg, which can have relatively lower voltage ratings, are implemented using Si-based MOSFETs with a blocking voltage of 100V to achieve cost advantages. Although Si MOSFETs have limitations in increasing switching frequencies compared to SiC MOSFETs, this choice is feasible because the current ripple in the buck leg is relatively lower than in the boost leg. Additionally, the boost-leg, which experiences a higher current ripple, employs 650V-rated SiC MOSFETs to increase switching frequency and reduce ripple. Furthermore, the two-parallel interleaved structure helps cancel the ripple in passive components, thereby reducing their required capacitance.

D.2. Optimized control design for Si-SiC Hybrid Interleaved Buck-Boost Y-Inverter

D.2.1 Modulation

Since the Y-inverter's Boost Stage has a higher current ripple than the Buck's leg, SiC MOSFET can be applied to the Boost Stage to reduce ripple strategically. In this study, we will discuss how to implement a three-phase motor system using Imperix B-Board, which has the potential to control high-speed switching to have dual switching frequency using Si MOSFET and SiC MOSFET.

The relationship between the input voltage and the output voltage of the buck converter and the boost converter may be expressed by the following equation

$$\frac{V_{abc.n}}{V_{pn}} = \frac{d_{BU}}{1 - d_{BO}} = \frac{d_{BU}}{d_{BOC}} = \frac{\hat{V}}{V_{pn}} \cdot [1 + sin(\omega_F t)] \qquad (D.1)$$

where, $V_{abc.n}$ represents an output capacitor voltage of each a-b-c 3 phase, and V_{pn} represents an input voltage. d_{BU} is the duty ratio of the buck converter, and d_{BO} represents the boost converter of a duty ratio, and d_{BOC} is its complementary (i.e., logic negation) signal.

Based on Eq. (D.1), various modulation strategies are, in principle, possible. For instance:

- Single-duty: if $d_{BU} = d_{BO} = d$, a single parameter modulation is achieved, with the diagonal switch-pairs in the H-bridge cell turned on and off jointly.
- Dual-duty: this is implemented by keeping separate variable duty cycles for the buck and boost cells and setting $d_{BU} = 1$ during boost-mode operational and, vice versa, $d_{BOC} = 1$ during buck-mode operation.
- Hybrid duty: by setting $d_{BOC} = k$ (with $0 < k < 1$) and using only d_{BU} as the control parameter, the boost-side leg transistors are operated with constant duty and the buck-side ones with variable duty. Of course, the possibility to also set a fixed d_{BU} value

and variable d_{BOC} also exists theoretically; however, for the case of sinusoidal modulation, the need to ensure $0 < d_{BOC} < 1$ implies some increased complication.

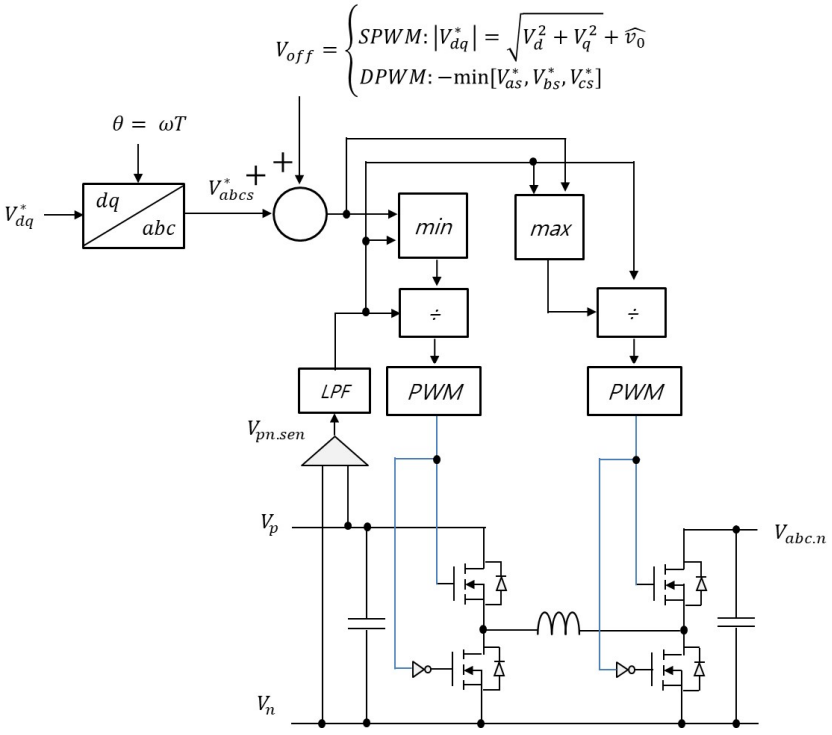
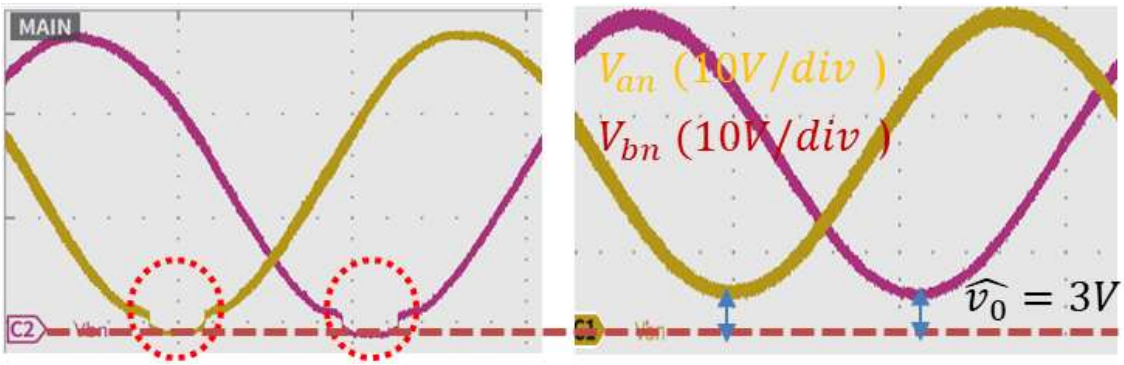


Figure D. 6. Cell circuit schematic and modulation diagram.

In this work, the *dual-duty* modulation approach is considered, with optimized different values of the switching frequency for the input and output switches, respectively.

In Figure D.6, V_{dq}^* is the command voltage required for the load phase voltage expressed in the *d-q* synchronous reference frame. The electrical angle (θ) can be obtained by multiplying the electrical angular velocity (ω) by the sampling time (T) and the three-phase command voltage from the *a-b-c* stationary reference frame (V_{abcs}^*). The calculated that three-phase command voltage requires the output capacitor voltage of each cell Buck-Boost converter with the magnitude of the command voltage as a DC offset to be applied to the load. Therefore, the offset voltage may be implemented by adding the magnitude of V_{dq}^* to each of the three-phase command voltages, as also indicated in Figure D.7. However, since errors in the practical implementation of the minimum voltage may occur due to

resistance and sensing errors of the capacitor, it may be additionally corrected by an additional arbitrary $\widehat{v_o}$ term. With this approach, sinusoidal PWM (SPWM) is implemented.



(a) (b)

Figure D. 7. (a) without arbitrary voltage (b) with arbitrary voltage of 3V.

Next to SPWM, discontinuous PWM (DPWM) is also considered to reduce the output capacitor voltage peak of the Y-inverter and increase voltage utilization, with an approach similar to Space Vector PWM with 3rd harmonic injection to the neutral point in a two-level VSI. That is also very effective to boost efficiency since switching is stopped for portions of the period. Here, specifically, a two-thirds discontinuous modulation (TTM) scheme was implemented.

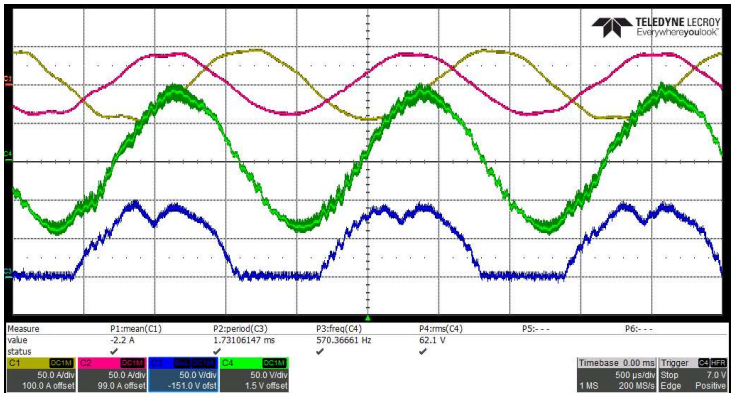


Figure D. 8. Experiment result in DPWM (red, yellow motor currents, green motor voltage and blue output filter capacitor voltage

D.2.2 Voltage and DC current sensor-less control

Figure D.9 provides a simplified representation of a typical DC/DC converter controller and motor current controller within a single-cell circuit. Ideally, the relationship between the duty cycle and output voltage in a DC/DC converter is linear, as shown in Equation (D.1). However, due to the inductor current and filter capacitor, practical considerations such as oscillations or delayed responses based on designed parameters must be taken into account. Therefore, most DC/DC converter controllers are designed in a cascade configuration, as illustrated in Figure D.10. This configuration is commonly used because DC/DC converters often employ a large DC link to maintain the DC voltage despite changes in output load. This helps rapidly respond to delays and oscillations.

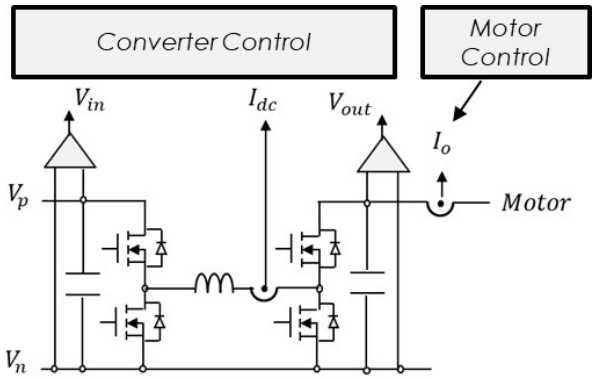


Figure D. 9. Cell circuit diagram with typical current controller for the motor drives with dc/dc converters.

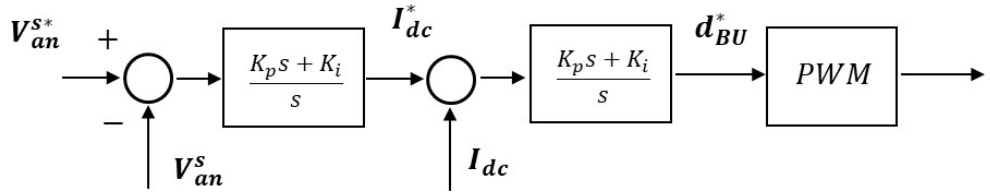


Figure D. 10. Typical voltage controller with cascade loop for DC/DC converters.

However, if the designed DC inductor and output capacitor have very small time constants and can respond quickly, the complex control structure shown in Figure D.10 can be disregarded. Specifically, if the control bandwidth of the DC/DC converter is 7 to 10

times higher than that of the motor control bandwidth, the response function of Figure D.10 can be assumed to be unity. In this case, the motor control can be implemented similarly to that of a typical VSI motor control. The PWM modulation technique introduced in Figure D.6 can then be adopted for control purposes.

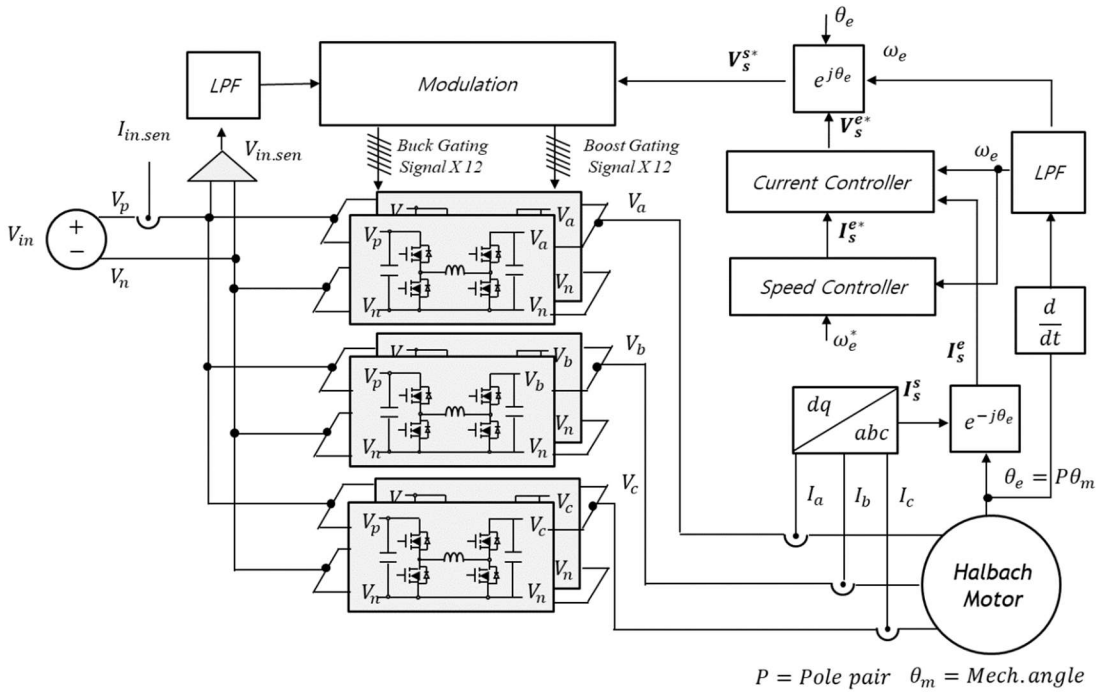


Figure D. 11. Overall control structure of interleaved Buck-Boost Y-inverter-fed three-phase ac motor driven system.

Therefore, under typical conditions, motor controllers can be designed using the FOC control method described in Section 5.1.2 without significant issues. However, in modular designs, fault scenarios must be considered. In modular systems, controlling each current separately increases the number of sensors required. This not only adds to the cost but also necessitates additional computational resources for the control design, further increasing expenses.

Voltage ripple cancellation and improved output voltage response were achieved by utilizing PWM with 180-degree phase shifts. However, if one of the interleaved modules fails to operate correctly, this advantage can be compromised, affecting only one of the

three motor phase voltages and leading to imbalance. This imbalance can cause delays in system control, resulting in a reduced control bandwidth. Under specific conditions, it may even lead to control deviating from the desired steady state.

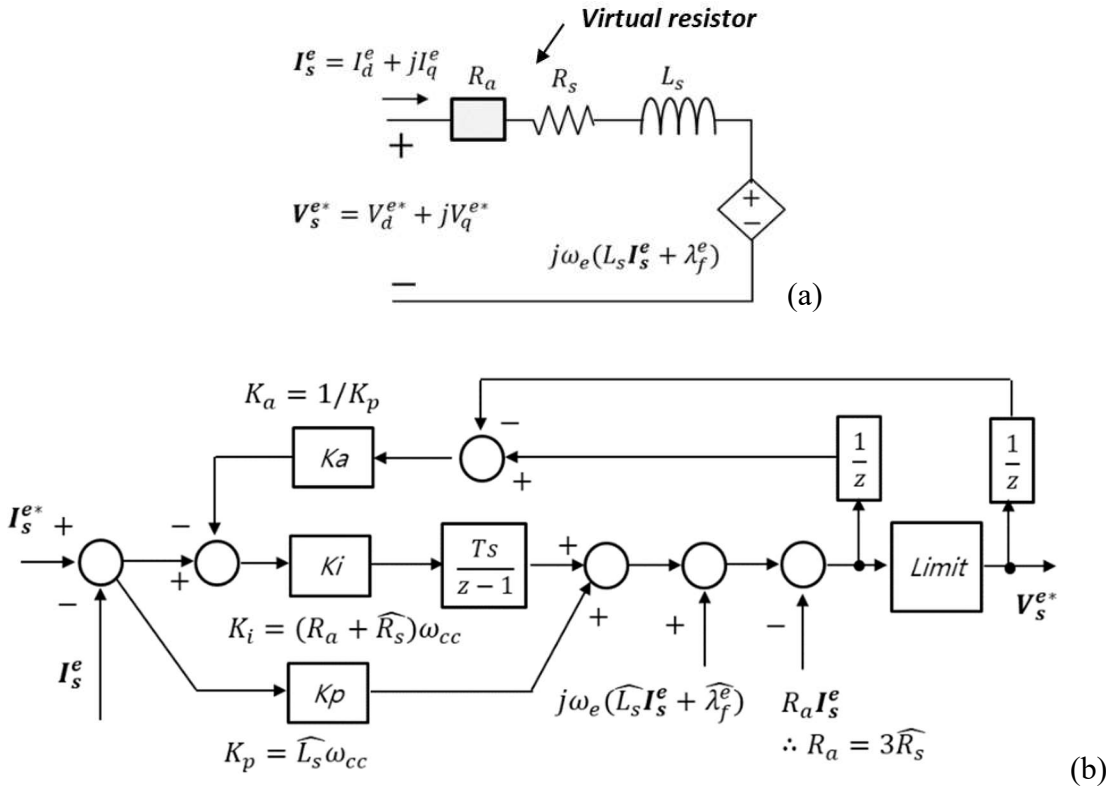


Figure D. 12. (a) Equivalent circuit of Y-inverter and AC motor with virtual resistor in the d-q synchronous reference frame; (b) block diagram of current controller with active-damping and anti-windup limiter.

Since each module lacks a current sensor, an effective way to address this issue is by implementing a virtual series resistor, as illustrated in Figure D.12(a), to enhance the responsiveness of the current and speed controllers. As explained in Section 5.1.1 of the main text, increasing the winding resistance of the motor decreases the electrical time constant and the electro-mechanical time constant, thereby accelerating the current response. Leveraging this advantage, it is expected to compensate for control delays due to imbalance.

To implement the virtual series resistor in the FOC current controller, it can be designed similarly to the conventional method, as shown in Figure D.12(b). The resulting controller can be expressed in Equation (D.2).

$$\begin{bmatrix} v_{ds}^{e*} \\ v_{qs}^{e*} \end{bmatrix} = \begin{bmatrix} \dfrac{K_{pd}s + K_{id}}{s} & 0 \\ 0 & \dfrac{K_{pq}s + K_{iq}}{s} \end{bmatrix} \begin{bmatrix} i_{ds}^{e*} - i_{ds}^{e} \\ i_{qs}^{e*} - i_{qs}^{e} \end{bmatrix} + \begin{bmatrix} 0 & -\omega_e \widehat{L_{qs}} \\ \omega_e \widehat{L_{ds}} & 0 \end{bmatrix} \begin{bmatrix} i_{ds}^{e} \\ i_{qs}^{e} \end{bmatrix} + \begin{bmatrix} 0 \\ \omega_e \widehat{\lambda_f^e} \end{bmatrix} - R_a \begin{bmatrix} i_{ds}^{e} \\ i_{qs}^{e} \end{bmatrix} \quad (\mathrm{D.2})$$

where L_{ds} and L_{ds} are the stator inductance, R_s is the stator resistance, R_a is the virtual resistance, λ_f^e is the motor magnetic flux linkage and the superscript e represents the synchronous reference frame. Additionally, in order to compensate for the decoupling term and back-emf voltage, the current controller considered the feed-forward term. The carat symbol (^) appearing above the coefficient variables denotes the estimated parameters. Similarly, the star symbol (*) above a value indicates it represents the desired value.

$$\begin{bmatrix} i_{ds}^{e} \\ i_{qs}^{e} \end{bmatrix} = \begin{bmatrix} \dfrac{K_{pd}s + K_{id}}{(L_{ds}s + R_s + R_a)(s + \omega_{cc})} & 0 \\ 0 & \dfrac{K_{pq}s + K_{iq}}{(L_{qs}s + R_s + R_a)(s + \omega_{cc})} \end{bmatrix} \begin{bmatrix} i_{ds}^{e*} \\ i_{qs}^{e*} \end{bmatrix} \quad (D.3)$$

$$\begin{bmatrix} i_{ds}^{e} \\ i_{qs}^{e} \end{bmatrix} = \frac{\omega_{cc}}{(s + \omega_{cc})} \begin{bmatrix} i_{ds}^{e*} \\ i_{qs}^{e*} \end{bmatrix} \quad (D.4)$$

The control gain values used in Equation (D.2) are illustrated in Figure D.12(b). If all parameters match precisely, the response will take the form of a first-order low pass filter, as shown in Equation (D.4).

D.3. Prototyping and demonstration of design

For the inverter, a hybrid approach was implemented, utilizing Si MOSFETs (Infineon IPT020N10N3) on the low-voltage input side and SiC MOSFETs (ROHM SCT3017ALHR) on the high-voltage output side. The input and output cells were switched at different frequencies, 50 kHz and 150 kHz, respectively, to optimize efficiency. Additionally, to meet power rating requirements, the inverter was constructed with interleaved cells, operating with a 180-degree phase shift between them. This method, as opposed to simply paralleling more semiconductor devices, reduces the size, volume, and weight of the inductor and output capacitor. The hardware prototype, along with the control board (Imperix B-Board), is shown in Figure D.13.

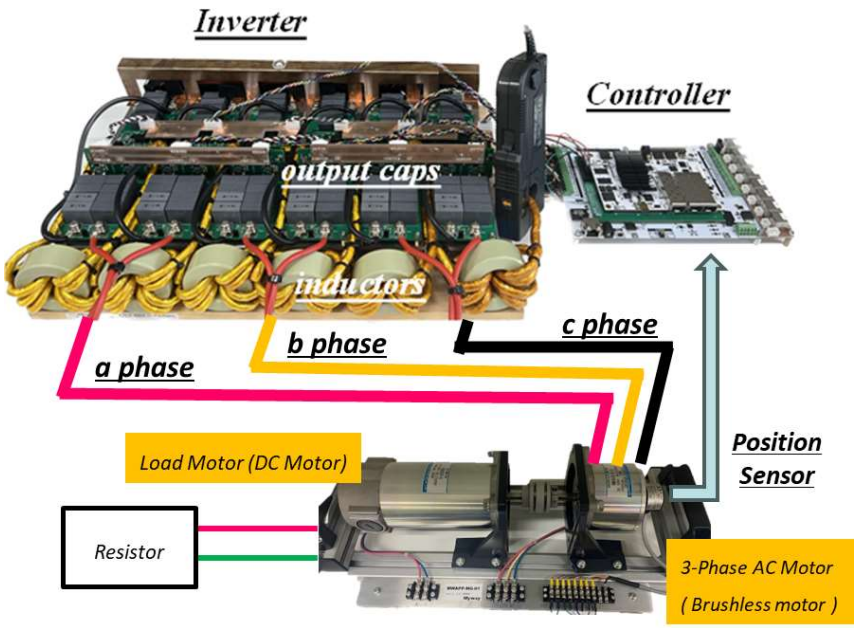


Figure D. 13. Prototype of 3-phase dual switching-frequency hybrid Si-SiC interleaved Y-Inverter with motor test bench and control board.

An experimental setup was established to assess the designed controller. A small brushless motor test bench was used, with parameters $L_s = 4\,mH$ ($L_d = L_q$) and $R_s = 0.9\,\Omega$, and a maximum nominal rotational speed of 2500 rpm. An incremental encoder (1024) was utilized for control purposes. To evaluate the controller's performance, one DC-

DC converter cell was intentionally removed from one of the interleaved legs of one phase (phase b), as seen in Figure D.14.

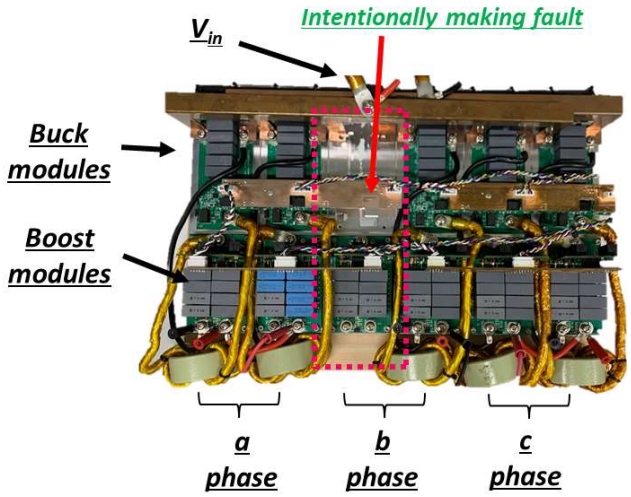


Figure D. 14. Intentionally failing one of the b-phase interleaved power module to create an imbalance condition.

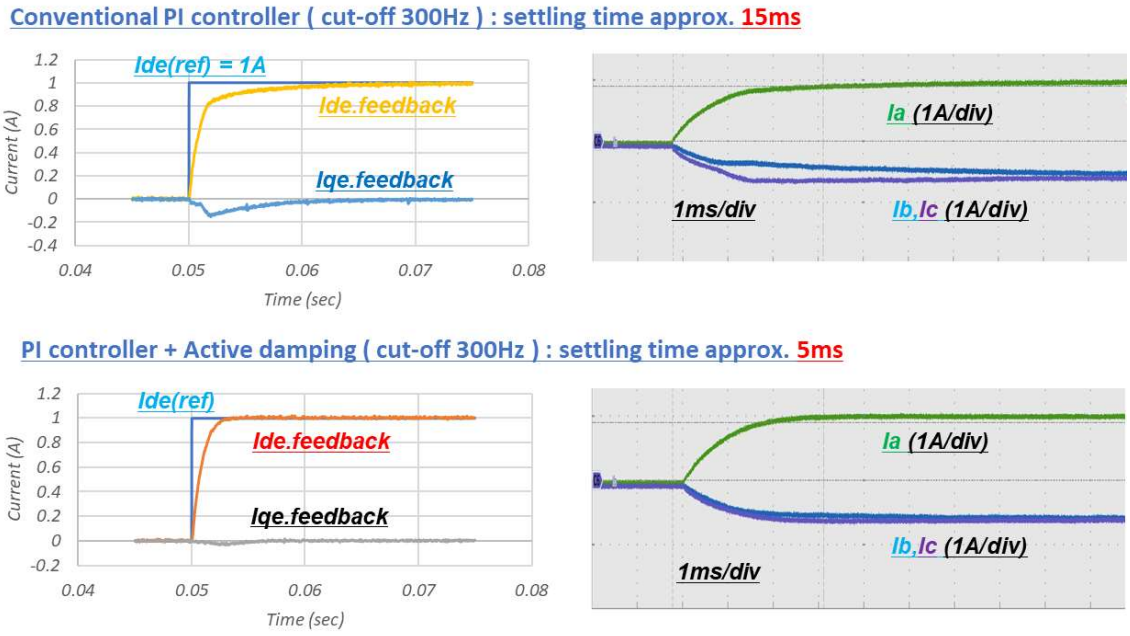
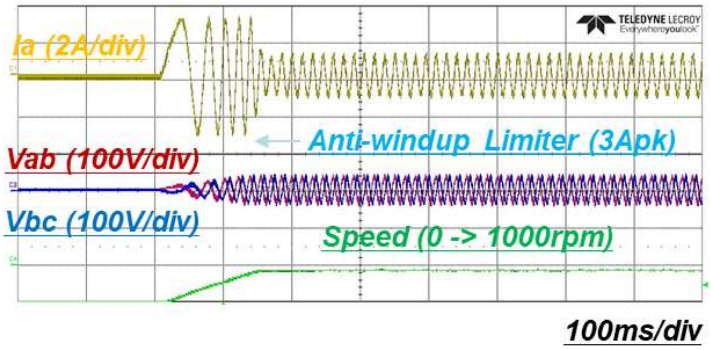
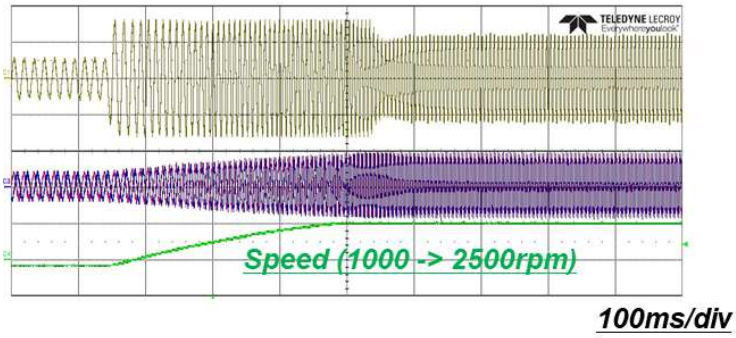


Figure D. 15. Step response of the current controller with unbalanced interleaved power module. (a) conventional PI control, (b) PI control with active damping method.

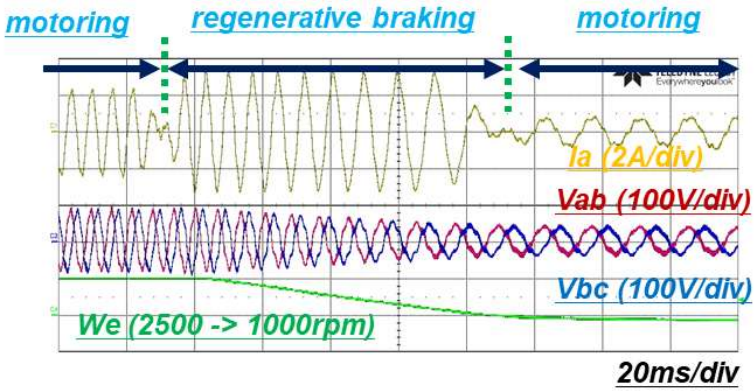
The dynamic response of the current controller was optimized using a DC current step response, as illustrated in Figure D.15. In (a), using a conventional controller, the target value was achieved after approximately 15ms. In contrast, in (b), employing active damping, the target value was attained within about 3ms, demonstrating a significant improvement (the cut-off frequency was set at 300 Hz).



(a)



(b)



(c)

Figure D. 16. Motor driving test with 1 kHz cut-off frequency of current control (a) startup response (0 →1000rpm), (b) speed up response with max. speed (1000 →2500rpm), (c) speed down response with regenerative braking control (2500 →1000rpm).

Figure D.16 summarizes some salient operational features of the system. In (a), the startup performance was validated, and the boosting function with an output voltage surpassing the input voltage was affirmed through maximum speed operation in (b). Moreover, as depicted in Figure D.16 (c), the Y-inverter inherently facilitates bidirectional power conversion, confirming the current controller's performance during regenerative braking control.

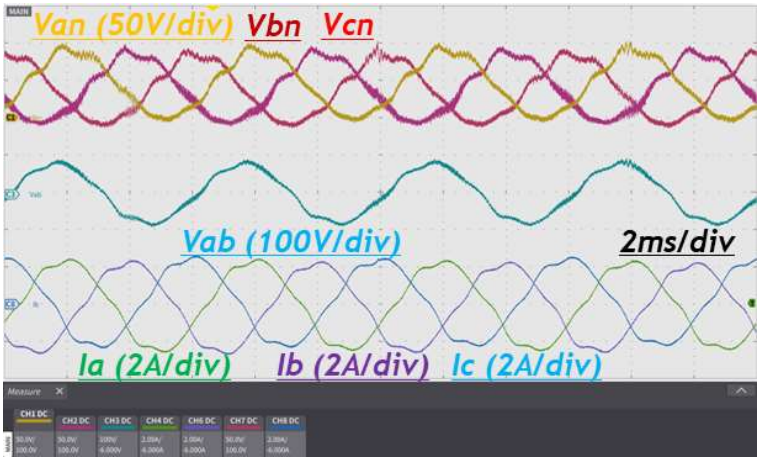
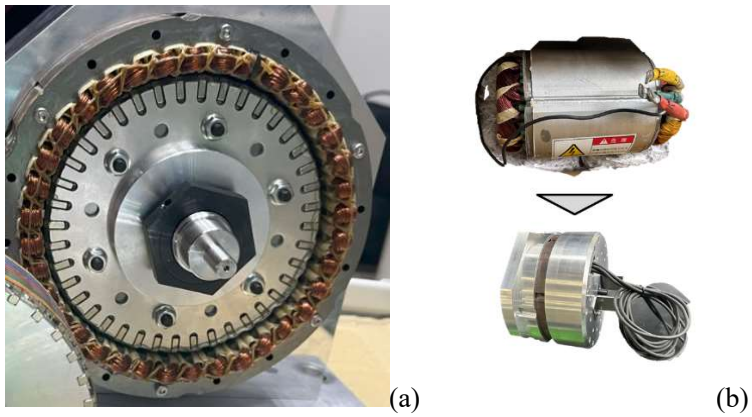


Figure D. 17. Output capacitor voltage of each phase, brush-less motor drive voltage and phase currents of the motor.

Furthermore, despite this significant asymmetry in the inverter structure, the controller ensured well-balanced operation, as demonstrated by the results in Figure D.17. It is evident that the ripple of the capacitor voltage in the b-phase is higher during buck operation, but the current of the three-phase motor is effectively regulated.



(a) (b)

Figure D. 18. Prototype of the Halbach motor: (a) detail of windings and Halbach rotor magnets; (b) Replaced the existing induction motor with a Halbach motor with enclosure for mounting and mechanical fixing to the EV car.

Figure D.18 shows the first machine prototype, which features a quantitative reduction of 50% weight and volume as compared with benchmark induction type machines designed for the same power rating and low voltage battery considered here of 60V.

Table D. 2. Y-Inverter - Halbach Motor Drive System Parameters

Motor Inductance (*Ls*)	42 uH
Motor Resistance (*Rs*)	0.0163 Ω
Back-emf constant (λ_f)	0.01646
Pole pair (P)	20
Sampling & Control frequency	50 kHz
Switching frequency	50 kHz (Buck-side) 150 kHz (Boost-side)
Cut-off frequency of current controller	1.5 kHz
Active damping gain (*Ra*)	3*Rs*

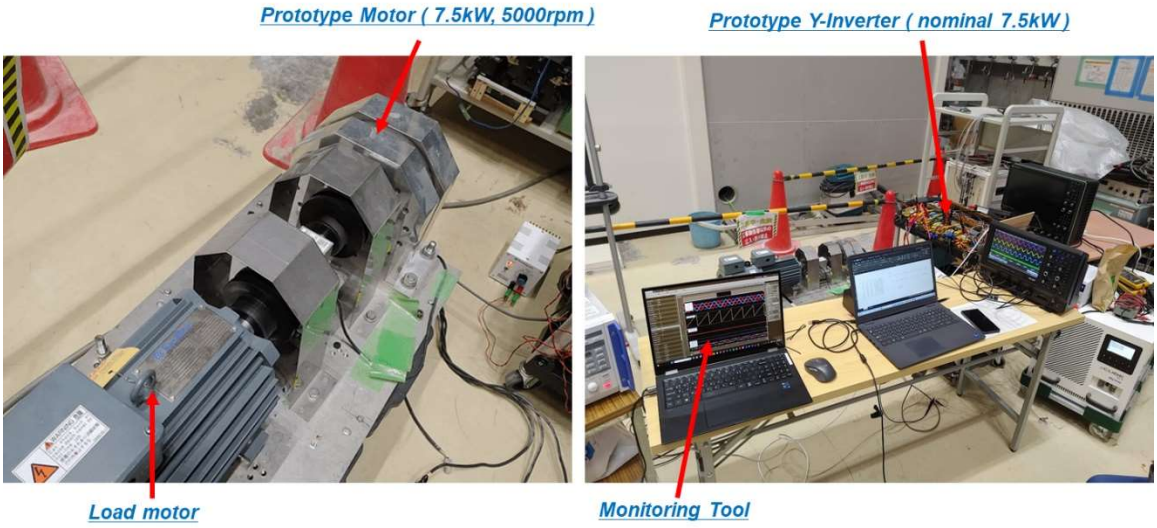
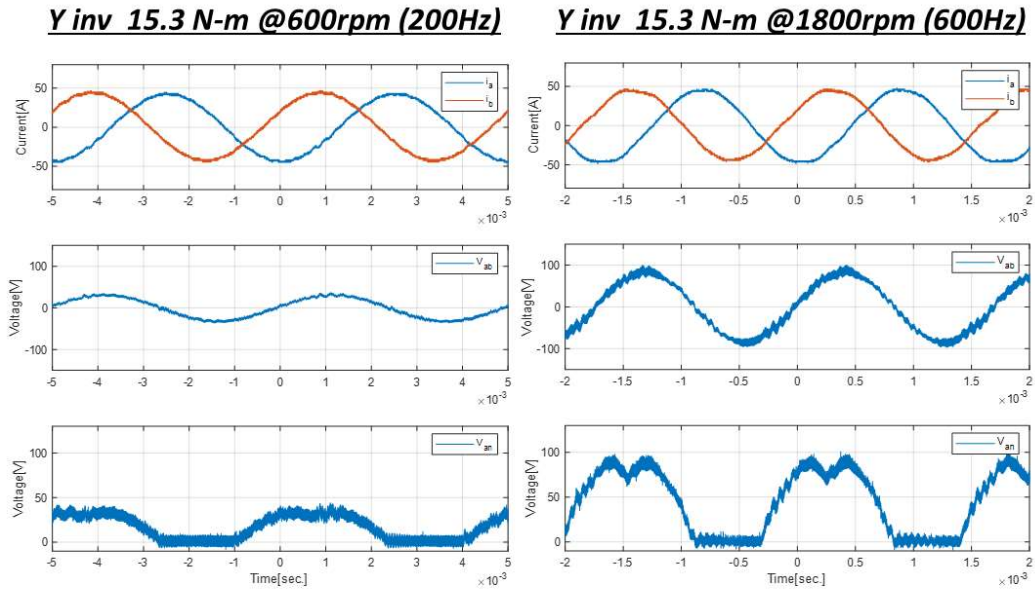


Figure D. 19. Experimental set-up with motor test bench for Y-inverter-fed Halbach motor.

Finally, the Halbach motor experimental setup shown in Figure D.19 was assembled and used for final characterization. Figure D.20 shows representative waveforms for DPWM, with test conditions of 15.3 N-m torque and motor rotational speeds of 600 rpm and 1800 rpm in (a) and (b), respectively. Under the same load torque, motor terminal currents were

approximately 30 Arms at different speed conditions, while the phase-to-phase motor voltage was close to an ideal sinusoidal waveform.



(a) (b)

Figure D. 20. Halbach motor terminal current (ia, ib), terminal phase-to-phase voltage (Vab), and buck–boost output capacitor voltage (Van): (a) 600 rpm (electrical 200 Hz) and 15.3 N-m load torque condition results; and (b) 1800 rpm (electrical 600 Hz) and 15.3 N-m results.

Figure D.21 displays the measured inverter efficiency under various torque and speed conditions. These measurements account for gate-driver losses, which are approximately 12 W. The maximum efficiency recorded, for power levels up to about 50% of the maximum rating, reached 97%. It is noteworthy that even under partial load conditions, the inverter maintained relatively high efficiency.

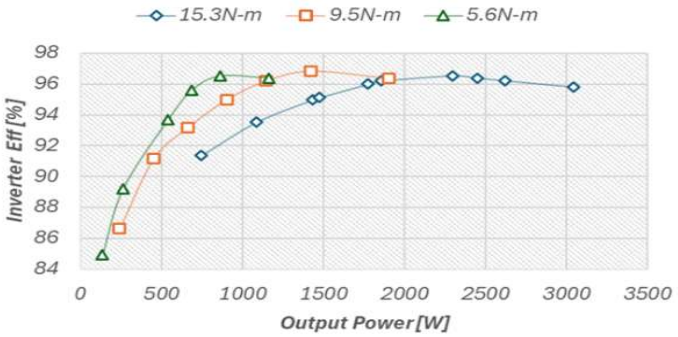
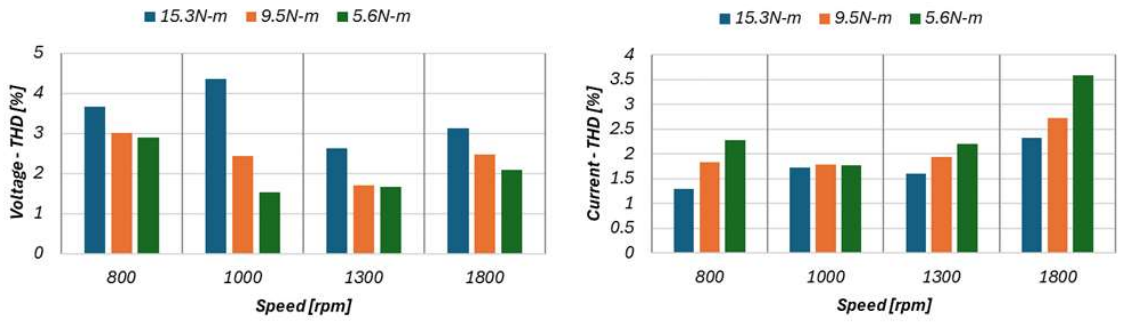


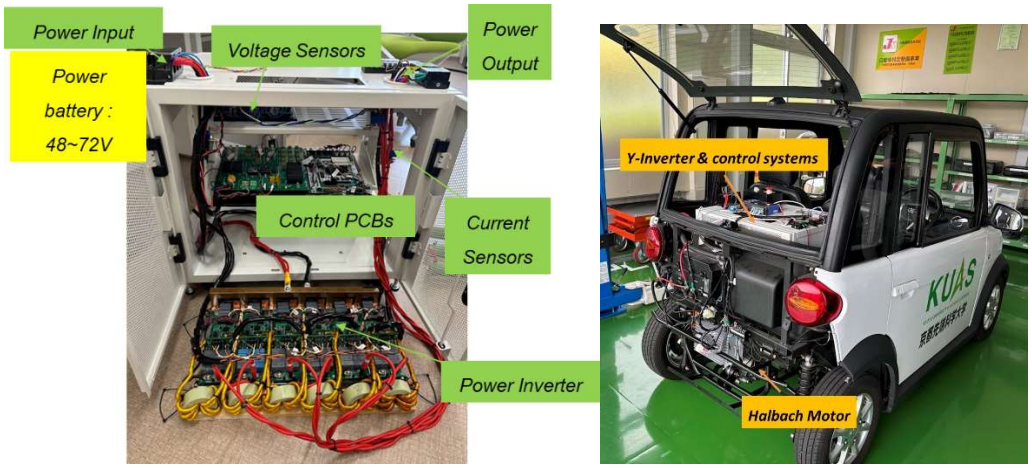
Figure D. 21. Inverter efficiency in the motor test bench with Halbach motor at various load–torque conditions.



(a) **(b)**

Figure D. 22. Measured total harmonic distortion under various load–torque conditions: (a) voltage THD; and (b) current THD.

Finally, Figure D.22 presents the measured harmonic distortion for the phase-to-phase motor terminal voltages and motor currents under various speed and load torque conditions. Both voltage and current total harmonic distortions remained below 5% across all test scenarios. These excellent results can be attributed to the combination of the inverter and the Halbach rotor machine design. Comparative tests conducted with a non-permanent magnet-type machine produced distinct harmonic profiles.



(a) **(b)**

Figure D. 23. (a) Prototype Y-inverter Control Box with sensors and additional controllers. (b) Practical demonstration of a Y-inverter driven EV car.

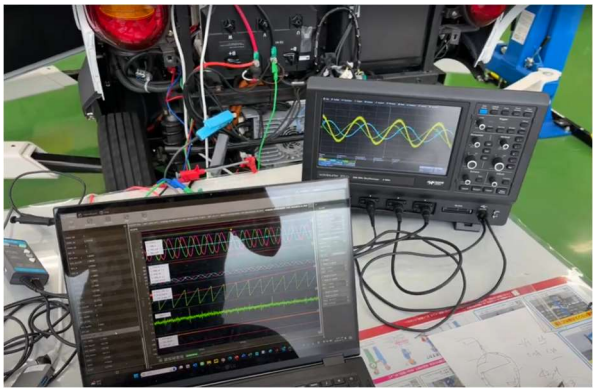


Figure D. 24. T**he preliminary experiment EV car operation powered by Y-inverter with the proposed controller.**

This study designed a motor controller for a modular design-based Y-Inverter with interleaved switching capability and validated it in an actual EV car. The control voltage of the motor was very close to sinusoidal, and common electrical noise was minimized. This development has undergone initial stage validation, and it is hoped that further research will reveal many advantages through comparative verification with other systems.