INVERTER-MACHINE PARAMETRIC CO-DESIGN FOR ENERGY EFFICIENT ELECTRIC DRIVE SYSTEM

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Abstract

This research paper presents an integrated design methodology for the inverter and motor that drive electric vehicles (EVs). As the demand for EVs increases, so does the necessity for research into developing energy-efficient electric drives comprised of inverters and motors. Advances in battery technology are pushing the industry towards the development of high-voltage EV systems, such as 800V systems, which require improvements in rapid charging technology, power density, and energy efficiency. This evolving landscape has sparked increased interest in Wide Band Gap (WBG) devices, particularly Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) as a replacement for traditional Silicon (Si) Insulated-Gate Bipolar Transistors (IGBTs). SiC-MOSFETs, with their low switching loss, high voltage ratings, and stability at high temperatures, enable high-speed switching, a feature difficult to achieve with Si-IGBTs due to thermal limitations. The paper proposes a comprehensive design strategy that leverages the advantages of these cutting-edge technologies, ultimately contributing to the advancement of efficient and high-performing electric drive systems for future EVs.

However, the move towards high-speed switching also introduces potential issues such as high dv/dt, which can be mitigated by employing techniques like multi-level topology. Among various multi-level topologies, the 3-level Active Neutral Point Clamped (3L-ANPC) topology is receiving substantial attention due to its high reliability and relatively stable loss distribution. While high voltage solutions increase the voltage applied to power devices, multi-level topologies like 3L-ANPC can address this problem by distributing voltage levels. Another benefit of the 3L-ANPC is its capability to implement various Pulse Width Modulation (PWM) strategies. The paper delves into multiple PWM strategies, emphasizing those aimed at energy loss optimization.

Interior Permanent Magnet Synchronous Motors (IPMSMs) are being extensively used in machines, offering advantages like high speed, power density, and stability. Since motors and inverters operate in a mutually influencing manner, it is vital to incorporate this interplay into the design considerations. The research presents a co-simulation model that takes into account the design parameters of both the motor and inverter to analyze system-wide energy loss. The ultimate goal is to use these representative operating points,

calculated from several standardized drive cycles, in order to design an electric drive that minimizes energy loss.

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Nomenclature

AC – Alternating Current

ANPC – Active Neutral Point Clamped

BEV – Battery Electric Vehicle

BFoM – Baliga's Figure of Merit

CCD – Central Composite Design

CHB – Cascade H-Bridge

DC – Direct Current

DOE – Design Of Experiment

EMF – Electro Motive Force

EV – Electric Vehicle

FC – Flying Capacitor

FEA – Finite Element Analysis

FFT – Fast Fourier Transformation

GaN – Gallium Nitride

HEMT – High Electron Mobility Transistors

IGBT – Insulated-Gate Bipolar Transistor

IPMSM – Interior Permanent Magnet Synchronous Motors

LC-PWM – Low Conduction Pulse Width Modulation

LS-PWM – Low Switching Pulse Width Modulation

LUT – Look-Up Table

MI – Modulation Index

MOSFET – Metal-Oxide-Semiconductor Field-Effect Transistor

NEDC – New European Drive Cycle

PF – Power Factor

PHEV – Plug-in Hybrid Electric Vehicle

PMSM – Permanent Magnet Synchronous Machine

PWM – Pulse Width Modulation

RSM – Response Surface Method

SBD – Schottky Barrier Diode

Si – Silicon

SiC – Silicon Carbide

SPWM – Sinusoidal Pulse Width Modulation

SVPWM – Space Vector Pulse Width Modulation

THD – Total Harmonic Distortion

VSI – Voltage Source Inverter

WBG – Wide Band Gap

WLTP – Worldwide Harmonized Light Vehicles Test Procedure

List of Symbols

A_F – Frontal area of Vehicle

B_g – Air-gap flux density

C_{rr} – Rolling resistance coefficient

C_d – Air-drag resistance coefficient

D_r – Rotor diameter

E_{crit} – Critical electric field

E_{cycle} – Energy loss during driving cycle

E_{on} – Turn-on switching loss

E_{off} – Turn-off switching loss

E_g – Energy band gap

ε_r – Dielectric constant

f_s – Switching frequency

F_a – Aerodynamic drag force

F_c – Climbing gradient force

F_{drive} – Driving force

F_m – Acceleration force

F_r – Rolling resistance force

g – Air-gap length

i_a – Phase current

i_d – d-axis current

i_q – q-axis current

i_C – Collector current

i_D – Drain current

k_c – Carter's coefficient

L – Inductance

L_d – d-axis inductance

L_q – q-axis inductance

l_{stk} – Stack length

m_a – Modulation index

m_f – Frequency modulation index

M_v – Vehicle mass

n – Doping density

n_i – Intrinsic carrier concentration

n_p – Number of poles

n_T – Number of series turns per phase

P_{cond} – Conduction loss

P_{CU} – Joule loss (Copper loss)

P_{ED} – Electric drive loss

P_{mag} – Magnet eddy current loss

P_{iron} – Iron loss

P_{sw} – Switching loss

q – Electric charge

R_a – Phase resistance

r_{on} – On-state resistance

R_{CE} – Collector-emitter resistance

R_{DS} – Drain-source resistance

R_F – Forward resistance

T – Torque

T_m – Magnetic torque

T_r – Reluctance torque

T_j – Junction temperature

TDR – Tire dynamic radius

V_{BD} – Breakdown voltage

V_{DC} – DC-link voltage

v_d – d-axis voltage

V_{LL} – Line-to-line voltage

v_{sat} – Saturation velocity

v_q – q-axis voltage

W_{drift} – Drift region thickness

β – Current phase angle

ρ – Air density

μ_0 – Vacuum permeability

μ_n – Electron mobility

ω_e – Electrical rotational speed

ω_m – Mechanical rotational speed

Ψ_m – Magnet flux

φ – Power factor

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1 Introduction

1.1 Background and Motivation

1.1.1 Sustainable Transportation

Efforts towards de-carbonization are ongoing across various industries in pursuit of sustainable development. One of the prominent sectors is the automotive industry, with the accelerated adoption of electric vehicles (EVs) being one of the primary strategies [1]. EVs offer a potent solution to reducing greenhouse gas emissions and achieving sustainable development. Unlike conventional internal combustion engine vehicles, EVs generate zero tailpipe emissions, contributing significantly to improving air quality, particularly in urban environments [2].

From a policy perspective, governments worldwide are actively promoting the use of EVs [3]. Incentives such as tax rebates, subsidies, and preferential policies, such as access to carpool lanes, are making EVs more attractive to potential buyers. The European Union has implemented new CO2 standards for cars and vans, in alignment with the objectives outlined in the 'Fit for 55' package for 2030. Meanwhile, in the United States, the Inflation Reduction Act (IRA), together with several states adopting California's Advanced Clean Cars II regulation, could drive electric cars to capture a market share of 50% by 2030, in line with the national objective. The introduction of the recently proposed emission standards from the US Environmental Protection Agency is expected to further boost this proportion. Some countries have even announced plans to phase out internal combustion engine vehicles entirely in the coming years. For instance, Norway is aiming for EVs to constitute 100% of its new-car sales by 2025. China's goal is to reach an annual EV sales target of 7 million by 2025, equating to approximately one-fifth of its domestic market demand. France, the United Kingdom, and California in the United States have declared their intentions to cease sales of vehicles powered by internal combustion engines by 2040. Figure 1.1 displays the target timeline for transitioning to zero-emission vehicles in various countries and the ban of internal combustion engine vehicles. Policies in these countries continue to evolve in favor of speeding up the adoption of EVs.

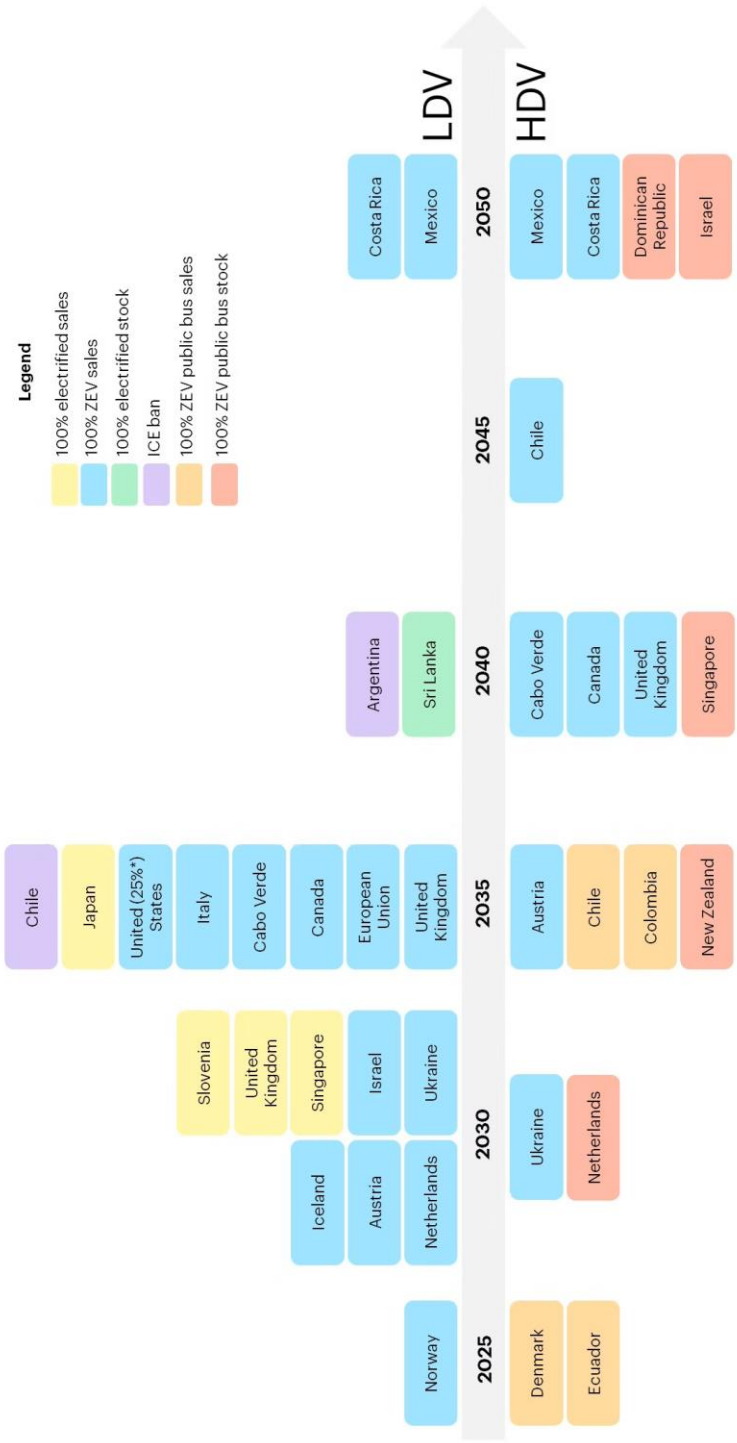


Figure 1.1. Global zero-emission vehicle mandate and internal combustion engine ban, from [3].

Note: ZEV: Zero emission vehicle, LDV: Light-duty vehicle, HDV: Heavy-duty vehicle

Moreover, the industry level is also demonstrating a commitment toward this transition. Automakers are investing heavily in EV technology and are expanding their EV offerings. Introducing more EV models across various segments creates greater choices for consumers, further boosting EV adoption. Tesla, one of the leading companies, has set a goal of producing 20 million EVs annually. General Motors has made a declaration to halt the sale of gasoline and diesel vehicles by 2035. Similarly, Toyota, a pioneer in hybrid vehicle technology, plans to roll out 70 electrified models by 2025, out of which 15 are expected to be battery electric vehicles (BEVs). Volkswagen, a traditional titan of the internal combustion engine vehicle industry, has stated that 2026 will be its final year to introduce a new internal combustion engine platform [4].

Owing to these policies and the active push for a shift towards EVs by automakers, predictions from the automobile industry suggest an eight-fold or greater increase in the EV fleet by 2030. This describes that the market for EVs is escalating at an average annual rate of approximately 30%. Figure 1.2 illustrates the forecast for the EV market under the declared policy scenarios and the Net Zero Emission 2050 scenario put forward by the International Energy Agency (IEA).

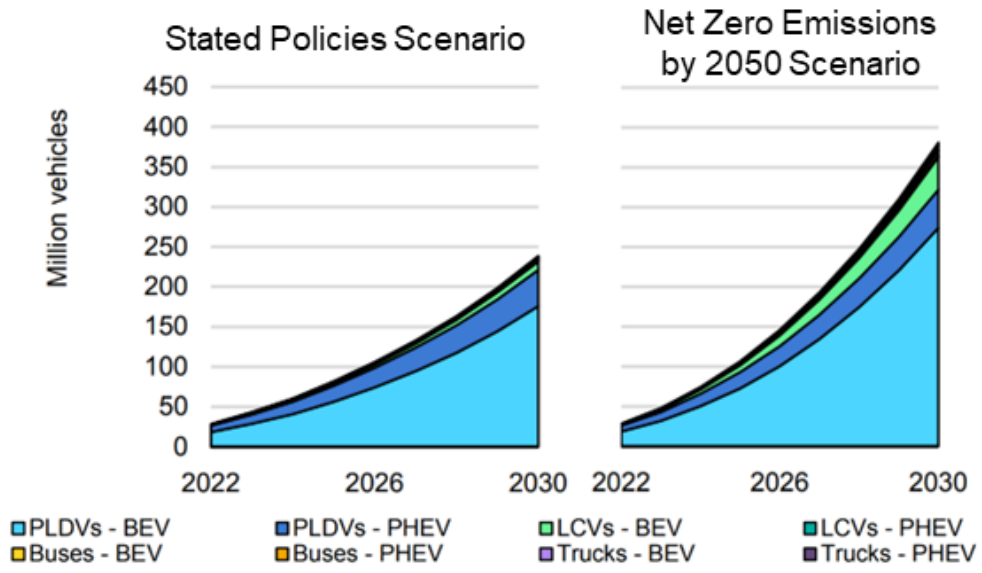
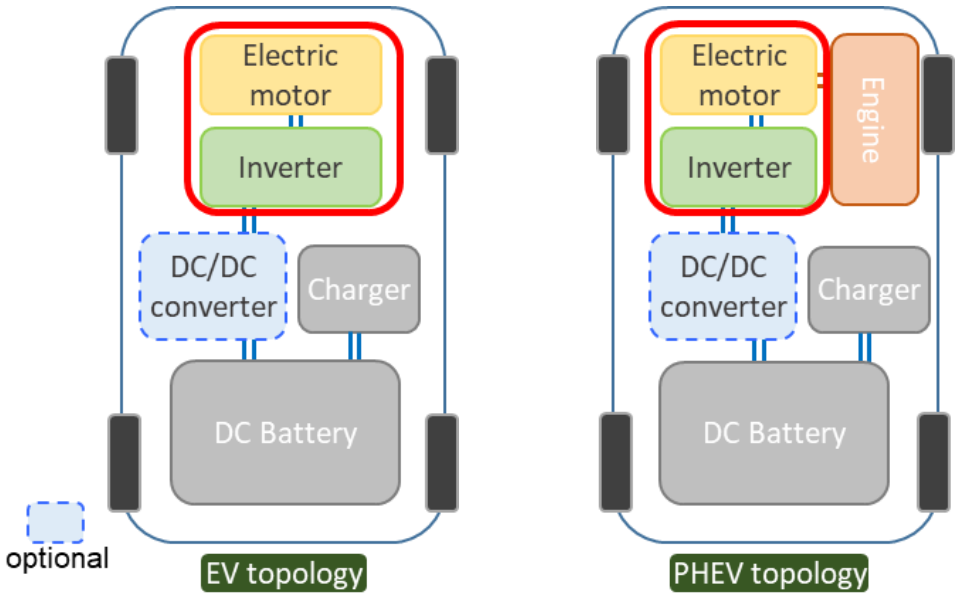


Figure 1.2. EV stock by different mode, 2022-2030, from [3].

Note: In order to meet the Net Zero Emissions 2050 target, set forth by the IEA, there is a need for a greater transition to EVs beyond what has been proposed in Stated Policies Scenario.
PLDV: Passenger light-duty vehicle, LCV: Light commercial vehicle, PHEV: Plug-in hybrid electric vehicle

1.1.2 Energy Efficient Electric Drive

The growing demand for EVs suggests a bright and sustainable future, however, there are still significant challenges to overcome. Some of the most prominent among these include the limited driving range offered by current battery technology and the need for a widespread and reliable charging infrastructure [5]. While improving battery technology is a crucial part of the solution, equal emphasis must also be placed on developing more efficient and powerful traction electric drives that can deliver better performance within the constraints of existing battery capabilities [6,7]. The traction electric drive system plays a pivotal role in determining an EV's performance, energy efficiency, and overall driving range – the key factors contributing to the EVs market success. When a high-power density electric drive is deployed, it allows for a decrease in the system's size and weight while maintaining or even increasing the output power. This attribute is particularly critical in the context of EVs, where both space and weight are of the utmost importance. A lighter and more compact drive system can lead to an increase in the vehicle's energy efficiency, thereby contributing to an enhanced driving range. Equally, high-efficiency design ensures that a large proportion of the electrical energy drawn from the battery is effectively converted into mechanical power for propelling the vehicle, rather than being wasted as heat. Drive systems with high efficiency not only reduce energy consumption but also extend the driving range and overall lifespan of the battery. Within the architecture of an EV, the traction electric drive majorly consists of the inverter and machine. Additionally, it encompasses elements such as gear reducers and, in certain situations, a DC-DC converter. Figure 1.3 provides a schematic representation of the topologies used in EVs and Plug-in Hybrid Electric Vehicles (PHEVs). The electric drive, which is the central focus of this study, is highlighted by the red line in this schematic. In summary, advancements in the design of traction electric drives are fundamental to overcoming the present-day challenges of electric vehicles. By leveraging such developments, strides can be made towards higher energy efficiency, increased driving range, and ultimately, a wider adoption of EVs.



(a) (b)

Figure 1.3. Schematics of (a) EV (b) PHEV and main components.

The inverter serves to convert the Direct Current (DC) power from the battery into Alternative Current (AC) power, which in turn drives the motor, ultimately propelling the vehicle. The precise design and operation of these two components are critical to the overall performance, efficiency, and driving range of the vehicle, thereby making them crucial areas of study in the advancement of EV and PHEV technology. Figure 1.4 provides an illustration of a traction electric drive system, which primarily consists of inverter, motor, and reducer [8].

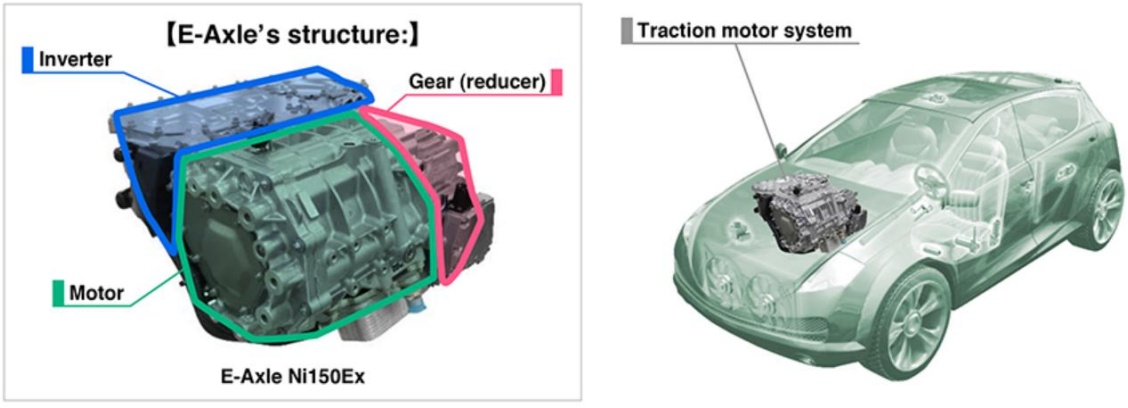
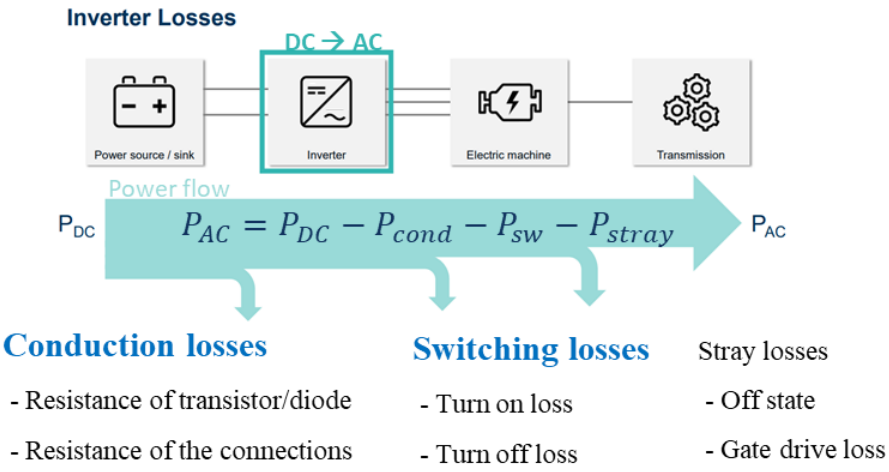
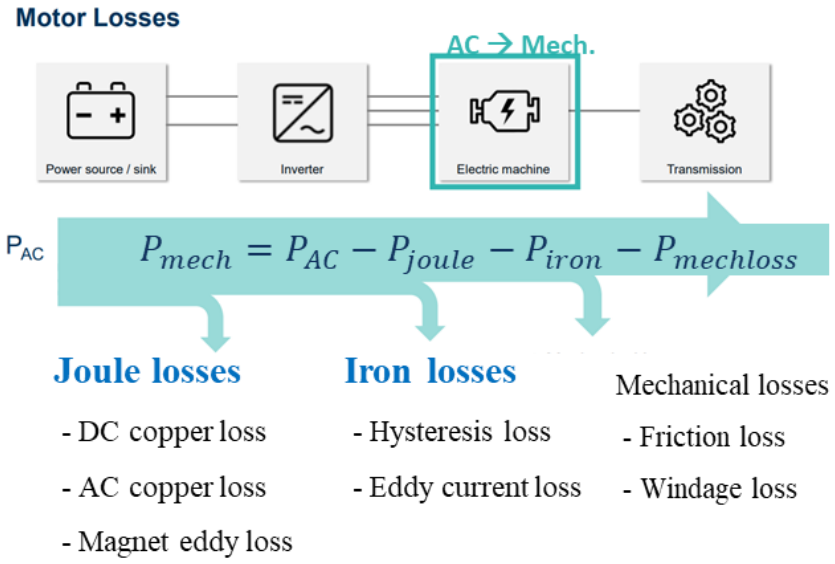


Figure 1.4. Nidec E-Axle: traction electric drive system, from [8].



(a)



(b)

Figure 1.5. Power flow and loss components of (a) inverter (b) motor in electric drive.

Figure 1.5 illustrates the primary energy losses that occur within an electric drive system. The process begins with a high-voltage battery supplying DC electrical input. This energy is then converted into an AC by the inverter to power a three-phase AC motor. During this conversion process, multiple forms of energy losses occur, including conduction losses, switching losses, off-state losses, and gate driver losses. Conduction losses arise due to the current flow within the inverter. Essentially, these are the losses experienced when electricity conducts through the semiconductor devices in the inverter.

Switching losses, on the other hand, are associated with the transition of power switches within the inverter. They occur as power devices switch on/off to generate the desired voltage waveform that drives the motor [9]. Further energy losses can be attributed to parasitic components during off-states and the operation of gate drivers. Off-state losses happen when the power devices in the inverter are not conducting but still lose a small amount of power due to leakage currents [10]. Gate driver losses are incurred when the gate drivers, which control the switching of the power devices in the inverter, operate [11]. The motor operates by receiving three-phase AC power, controlled by the inverter, and transforms it into mechanical power. During this transformation, several forms of energy losses occur. One of these is Joule losses, which encompasses copper losses and magnet eddy losses in the case of a Permanent Magnet (PM) motor. Copper losses is generated from the current flowing through the motor's wire. Additionally, iron loss occurs due to changes in flux within the magnetic core. Furthermore, mechanical loss, originating from the friction generated by the rotation of the motor, impacts energy efficiency. Factors influencing mechanical loss include the rotor size, its cooling method, and connected parts such as bearings. Interestingly, the direction of energy flow reverses when generating power to charge a battery in an electric drive, but the components involved remain the same. In this study, significant energy loss components are focused on analyzing for an energy-efficient electric drive design, highlighted in blue in Figure 1.5. These components include conduction losses and switching losses for the inverter, as well as Joule losses and iron losses for the motor. Understanding and minimizing these losses are critical steps in enhancing the overall efficiency of electric drive systems.

1.2 Co-design of Inverter-Machine

1.2.1 Interaction between Inverter and Machine

Inverters and machines in electric drives do not operate in isolation; rather, they interact significantly with each other. While the losses of inverters and machines can be calculated separately as discussed in the previous chapter, it is important to consider the influence they exert on each other's parameters. When evaluating and designing a machine, the ideal sinusoidal current could be used to analyze it for the sake of computational

efficiency. However, this can result in significant discrepancies in terms of loss prediction, particularly in high-speed regions where frequency impacts are substantial. Machine losses can considerably vary depending on the pulse-width modulation (PWM) control performance determined by the inverter. Therefore, it is essential to estimate motor losses, considering PWM. Figure 1.6 illustrates the current waveform based on the inverter's PWM switching frequency, the change in the machine's flux density, and the results of the iron loss analysis in relation to the switching frequency. As the PWM switching frequency is increased, the high-frequency harmonic component linked to the machine core's flux density change diminishes. As the current waveform becomes closer to the sinusoidal shape due to the increase in PWM switching frequency, this results in a decrease in iron losses. thereby enhancing the overall efficiency of the electric drive system. However, in the inverter, an increased switching frequency leads to greater switching losses in power device. Thus, to maximize the efficiency of the entire electric drive system, it is imperative to design an optimal switching frequency.

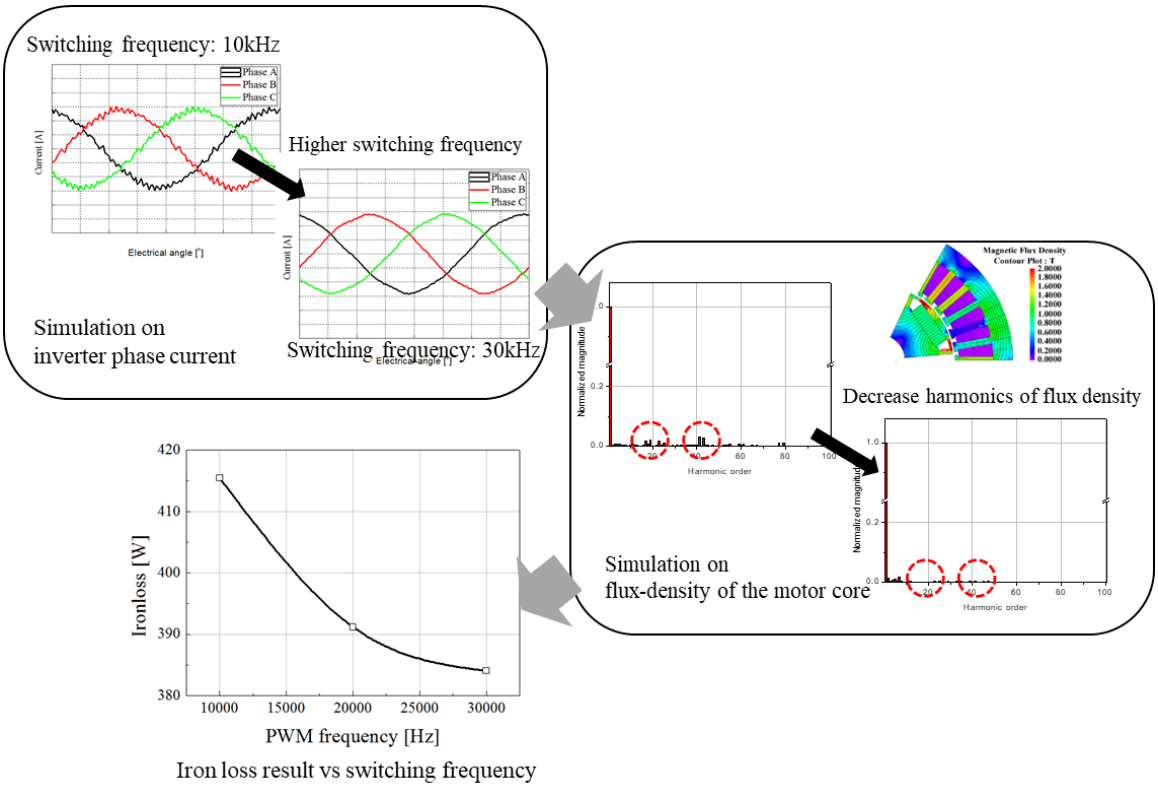
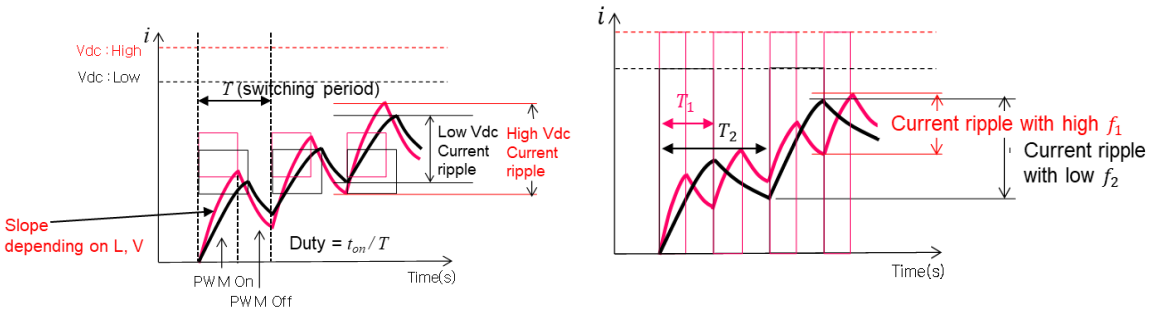


Figure 1.6. Iron loss analysis of the machine considering inverter PWM switching frequency.

Moreover, fluctuations in the motor back electromotive force (EMF) exceeding voltage limits, or significant voltage instability due to high harmonic content, can reduce the inverter's control performance. Thus, if the inverter losses are analyzed based on an ideal machine model, the estimation can deviate significantly from the actual scenario. Many studies have been conducted to analyze system losses, compensating for these issues [12-14]. However, research on designing the parameters for inverter and machine from the initial design stage, considering their interaction, is still limited. In industrial contexts, work towards the optimal design of each inverter and machine is actively progressing. Yet, design considerations taking into account the parameters of the inverter and machine and their co-effect are often overlooked. Consequently, this study aims to propose a co-design methodology that considers the interaction between the inverter and machine from the initial design stage and to demonstrate the potential improvements this can bring.

1.2.2 Necessity of Co-design

In typical scenarios, the output current of an inverter, serving as the input current of a motor, is sinusoidally modulated to the required frequency and magnitude to drive an AC motor. During the duty ratio D —defined as the on-time t_{on}, per switching cycle T— the current increases, then deflates for the remainder of the time. The adjustment of the duty ratio allows for the formation of the desired current waveform. However, this process invariably gives rise to current ripple. This ripple not only diminishes the efficiency of the motor but also influences vibration and noise performances [15]. Figure 1.7 illustrates the current ripple due to DC-link voltage, switching frequency, and motor inductance. As demonstrated in (a), the larger the input DC voltage of the inverter and the smaller value of the motor inductance, the larger ripple value, as indicated by the red current line. Furthermore, as shown in (b), augmenting the switching frequency—or equivalently, shortening the switching period—can reduce the current ripple under given voltage and inductance conditions. The approximate relationship between the current ripple and each parameter can be expressed through Equation. 1.1, where f_s represents the switching frequency, V symbolizes the voltage applied to the power device or the input voltage, and L is the motor inductance value.



(a) (b)

Figure 1.7. Current ripple depending on (a) V and L; (b) f_s.

$$i_{ripple} = \frac{1}{L}\int_0^T Vdt \qquad \text{Equation 1.1}$$

For an energy-efficient electric drive system, it is imperative to minimize the current ripple value, which is substantially influenced by inverter parameters like switching frequency and voltage and the motor parameter inductance. Thus, for optimal system efficiency, a design that reduces current ripple must simultaneously consider these parameters. Figure 1.8 displays the result of an excessive increase in magnet eddy current loss at high speeds due to an unintended current ripple value. This occurs when the design does not sufficiently consider current ripple, resulting in compromised motor performance and damaged reliability due to heat in durability tests. This problem can be resolved by increasing the inverter's switching frequency as displayed in Figure 1.9, which helps reduce the eddy current loss. Additionally, as can be seen in Figure 1.10, this also resolved by re-designing motor for increasing motor inductance. However, a superior outcome can be achieved by proceeding with an optimal design considering both motor and inverter design parameters at the initial design stage. This shows the importance of co-design at the inception of inverter and machine design processes. The implementation of energy-efficient electric drive designs can be more economically and efficiently achieved utilizing co-design methodology. Consequently, in this study, a co-design methodology that combines the most recent advancements in the realm of inverters and machines for electric drives is proposed, and the efficacy of these innovations is discussed.

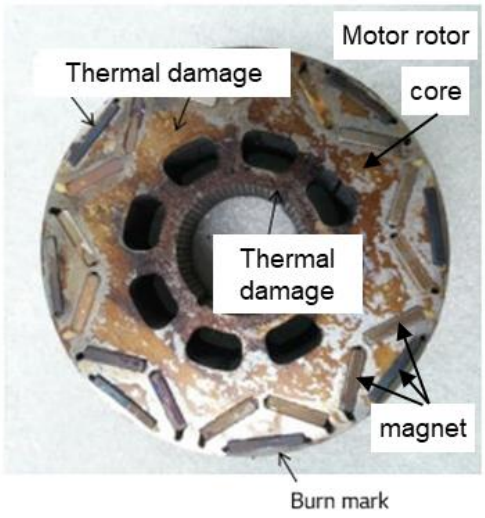


Figure 1.8. Heat damage during high-temperature operating durability test due to excessive magnet eddy current loss by unintended current ripple.

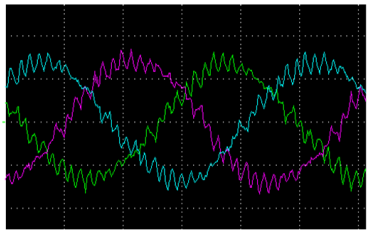
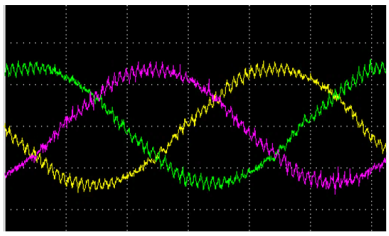
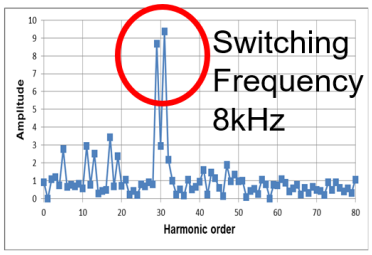
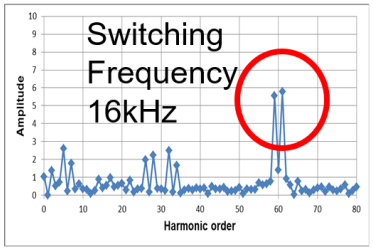
Switching frequency	8kHz	16kHz
Current measurement		
FFT* results (Harmonics)		
Magnet eddy loss[W]	215.5	151

Figure 1.9. Magnet eddy current loss analysis results depending on inverter switching frequency.

Note: Using double switching frequency from 8kHz to 16kHz, total magnet eddy current loss is reduced from 215.5W to 151W.

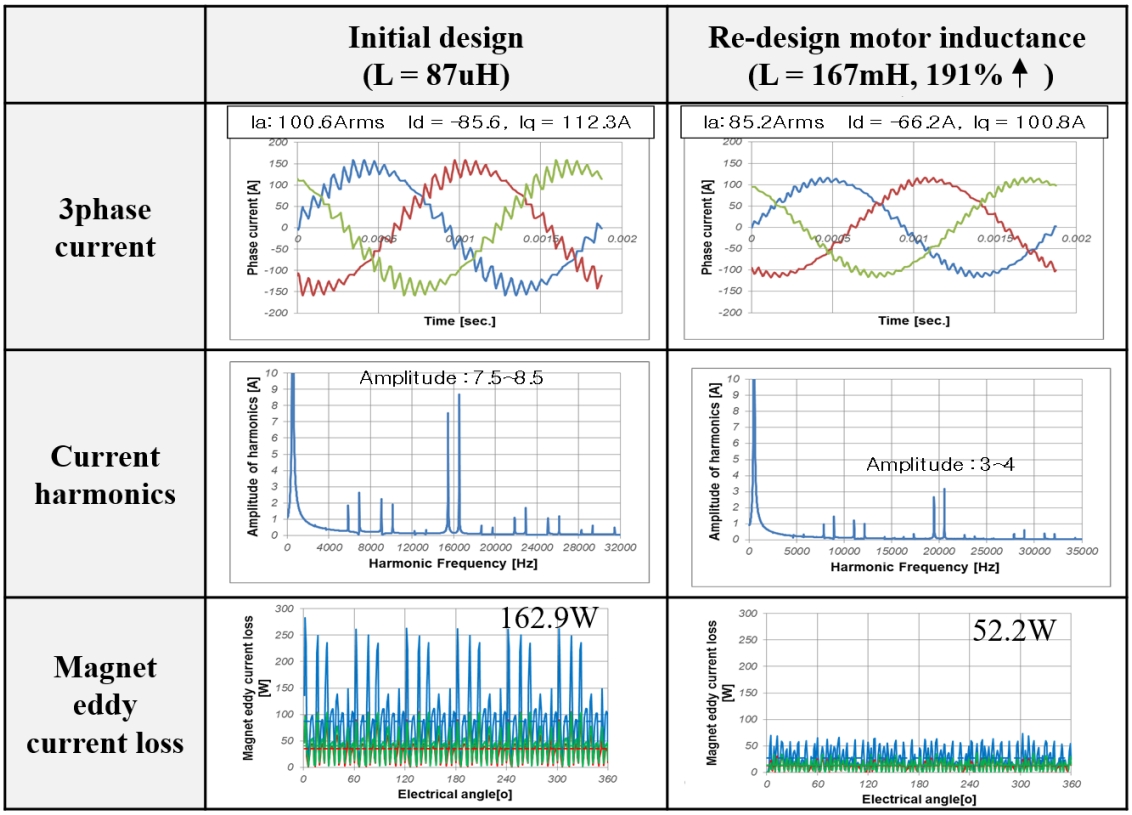


Figure 1.10. Magnet eddy current loss analysis results depending on motor inductance.

Note: Re-designing motor inductance from 87μH to 167μH by increasing stator turns, total magnet eddy current loss is reduced from 162.9W to 52.2W.

1.3 Thesis Outline

The full structure of the thesis is as follows.

Chapter 2 delves into the state-of-the-art technology trends related to energy-efficient electric drives. Research on inverters using wide-band gap (WBG) devices such as Silicon Carbide (SiC) or Gallium Nitride (GaN), suitable for high-speed applications, is actively being pursued. This chapter explores the unique properties of each WBG material and representative devices, and compares the merits and demerits of traction inverters, particularly from an energy perspective, against conventional silicon (Si) devices. Additionally, various multi-level topologies are discussed, with a specific focus on the topology and modulation techniques of 3-level Active Neutral Point Clamped (3L-ANPC).

The chapter concludes with a review of research on high-speed, highly efficient machine technology.

Chapter 3 addresses the methodology and process involved in designing energy-efficient electric drive system. Standardized drive cycles and their conversion into electric drive profiles are discussed, with innovative approaches proposed for the selection of representative load points for design considerations. Analytic loss calculations of each inverter and machine losses are included in this chapter.

In chapter 4, the computer-aided parametric co-design methodology is discussed. The detail description of co-simulation model specifically developed for this research is presented. A novel improving design method for designing inverters and machines based on this co-simulation model is introduced. The energy-efficient inverter design utilizing WBG devices and 3L-ANPC topology is proposed, demonstrating that this improved inverter design can yield substantial enhancements in the machine design. With high-speed switching, increasing pole numbers of the machine results in overall boost in system efficiency. Additionally, an improved machine inductance design that takes into account the impact of inverter parameters is discussed, that enables to enhance the efficiency and functionality of the system.

Chapter 5 contains a case study executed using industry-standard models and the methodologies outlined in the previous sections. Simulation results indicate a marked reduction in the total energy consumption over the course of the drive cycle, underscoring the efficacy of the approaches discussed in this study. The case study first delves into the application of a Belt-driven Integrated Starter Generator (B-ISG) in the 400V PHEV system. This is followed by an analysis of the improved design outcomes for an 800V BEV traction system. Finally, based on comparison energy consumption results of the two PWM strategies, a novel idea using hybrid modulation strategy is presented.

In chapter 6, the experimental demonstrations that lend support to the study is focused on. The experimental concept and setup are elaborated upon, with corresponding results for each variable presented. Improved results are generated and showcased through the fabrication and testing of a working prototype.

In chapter 7, the results and findings of the research is summarized and the contribution to the field is discussed. Potential avenues for future enhancements and advancements are presented.

2 Trends in State-of-the-Art Electric Drives

As discussed in chapter 1, vehicle electrification has been gaining momentum at a swift pace. This rapid progression, experienced over recent years, coincides with a transformative societal shift in transportation, characterized by autonomous mobility and service-driven conveyance, resulting in an expanded sphere of movement. These paradigm shifts instigate the demand for higher power and more efficient electric traction drive systems, thereby enabling enhanced fuel economy for a given battery charge. The U.S. Department of Energy, in conjunction with the U.S. Council for Automotive Research, has crafted a roadmap for electric passenger vehicles projected to 2025 [16]. According to this, a target power density of 33kW/L for a 100kW traction drive, a lifespan of 300,000 miles and 15 years, and a cost of $6/kW are presented for the development of a passenger car platform for high efficiency, compactness and economy. For the inverter, the objectives are a power density of 100kW/L and a cost of $2.7/kW, while for the motor, the power density aim strands at 50kW/L and the cost target at $3.3/kW. These overall aims constitute a daunting objective to curtail costs by 25% and reduce volume by 88% relative to 2020 figures. To fulfill these aims, numerous investigations into inverters and motors have been undertaken [17]. In this chapter, building on a comprehensive literature review, the most recent advancements in efficient electric drive technologies that facilitate the transition to EVs are discussed and elaborated upon.

2.1 Multi-level Inverter Topology

2.1.1 Conventional Two-level Inverter Topology

Traction inverters for EVs are dominated by two-level three-phase voltage source inverter (VSI) topology because of its high efficiency, simple control requirements, and low cost [18]. This inverter topology is presented in Figure 2.1. A pair of half-bridges, each made up of two power devices, is linked to each phase of the motor. In this each leg, the top and bottom switches (S1 and S2, S3 and S4, S5 and S6) operates in complementary, and it’s critical to ensure they are never switched on simultaneously. Otherwise, a short-circuit would occur on the input DC link, leading to possible system malfunction or damage. Additionally, the DC-link capacitors (C1, C2) are positioned at the input terminal of the

inverter on the side connected to the traction battery. A boost converter can be integrated between the DC input and the inverter. This converter serves to step-up the input DC voltage to the desired level before it is connected to the inverter [19]. This ensures that the voltage delivered to the inverter aligns with its operational specifications, enhancing the overall efficiency and functionality of the system.

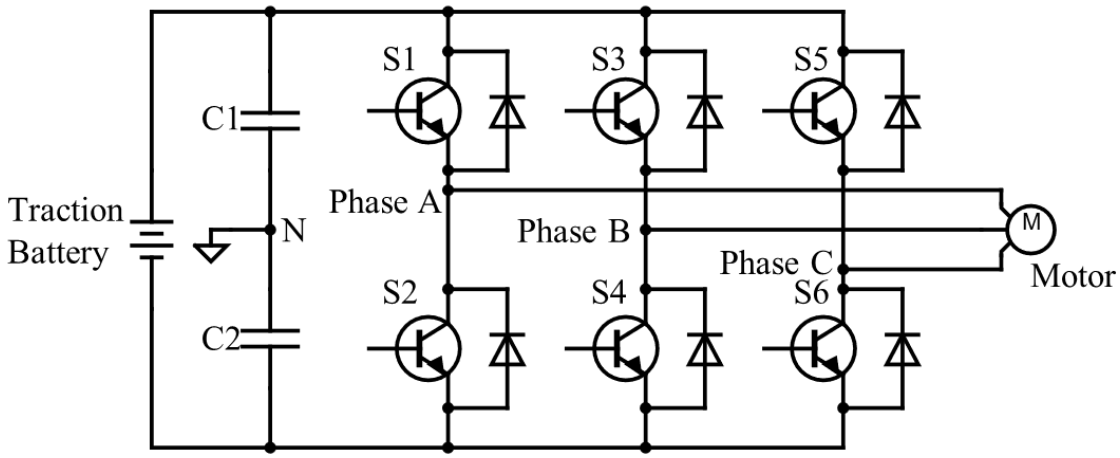


Figure 2.11. Typical two-level three-phase VSI topology

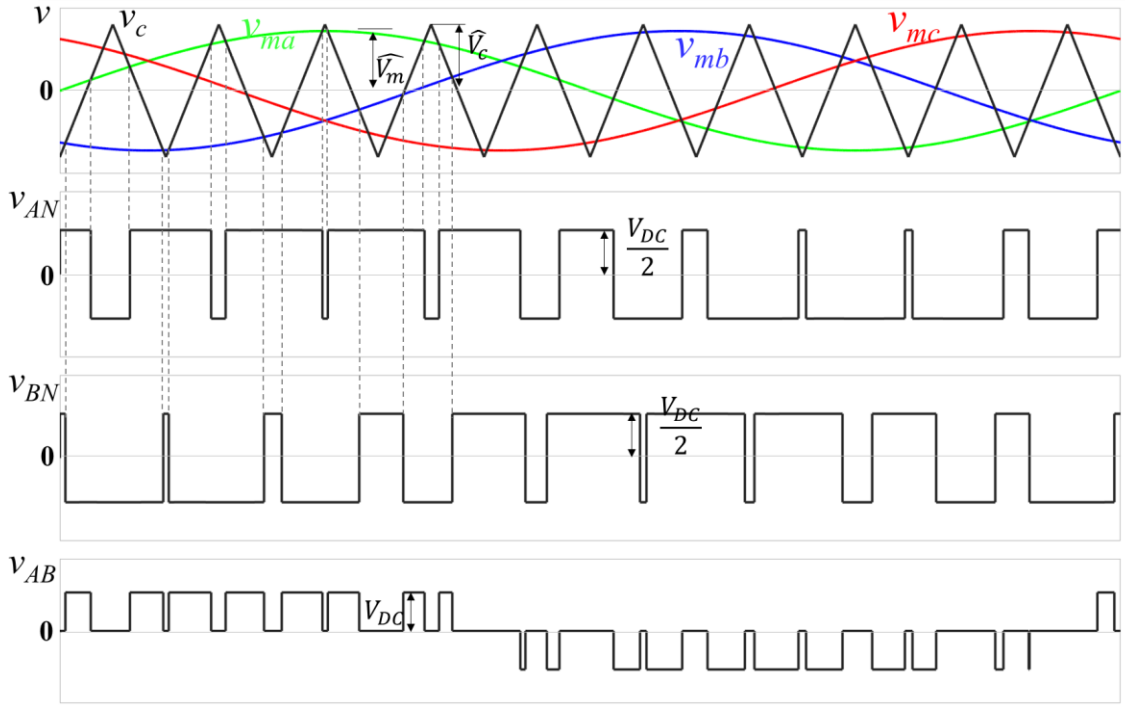


Figure 2.12. Typical Sinusoidal PWM for a two-level VSI

The general operation of a typical Sinusoidal PWM (SPWM) scheme for a two-level VSI is depicted in Figure 2.2. In this illustration, v_{ma}, v_{mb}, and v_{mc} represent the three-phase sinusoidal modulating waves, and v_c signifies the carrier wave. The fundamental-frequency component present in the output voltage of the inverter can be effectively regulated by the amplitude modulation index (MI), as defined in Equation 2.1. The role of the amplitude modulation index here is crucial as it manipulates the fundamental output voltage by adjusting the ratio between the peak amplitude of the modulating waveform, $\widehat{V_m}$ and the peak amplitude of the carrier waveform, $\widehat{V_c}$. Therefore, through the careful calibration of the amplitude modulation index, the operation and performance of the VSI can be optimized.

$$m_a = \frac{\widehat{V_m}}{\widehat{V_c}} \qquad \text{Equation 2.2}$$

The frequency modulation index is defined as represented by Equation 2.2, where f_m and f_c refer to the frequencies of the modulating and carrier waves. A higher number of m_f, which corresponds to a higher carrier frequency, results in enhanced control performance. This is due to the output wave being more closely aligned with the desired waveform.

$$m_f = \frac{f_c}{f_m} \qquad \text{Equation 2.3}$$

When the modulating signal exceeds the carrier signal, the switch S1, which is top switch of the A-phase leg is turn-on, and consequently, the bottom switch S2 is turn-off. As a result of this, v_{AN}, the phase-to-neutral voltage, becomes equivalent to $+V_{DC}/2$, where V_{DC} denotes the DC-link voltage. Conversely, if the carrier signal exceeds the modulating signal, S1 is turn-off while the S2 is turn-on. Consequently, v_{AN} transitions to $-V_{DC}/2$. Sice the waveform of v_{AN} has only two levels, $+V_{DC}/2$ and $-V_{DC}/2$, the inverter is known as a two-level inverter. A similar control mechanism is also employed for the other phases, ensuring smooth and efficient operation of the inverter. The line-to-line voltage vAB is determined by Equation 2.3.

$$v_{AB} = v_{AN} - v_{BN} \qquad \text{Equation 2.4}$$

Figure 2.3 presents a set of simulated waveforms for the two-level VSI, where v_{AO} is the load phase voltage, v_{AB} is the line-to-line voltage, and i_A is the load current. The

simulation conditions are f_m =100Hz, m_f =15, m_a =0.9, v_{DC} =400V, and loads are comprised by three-phase resistance-inductor (R-L), where *L*=20mH, *R*=20Ω.

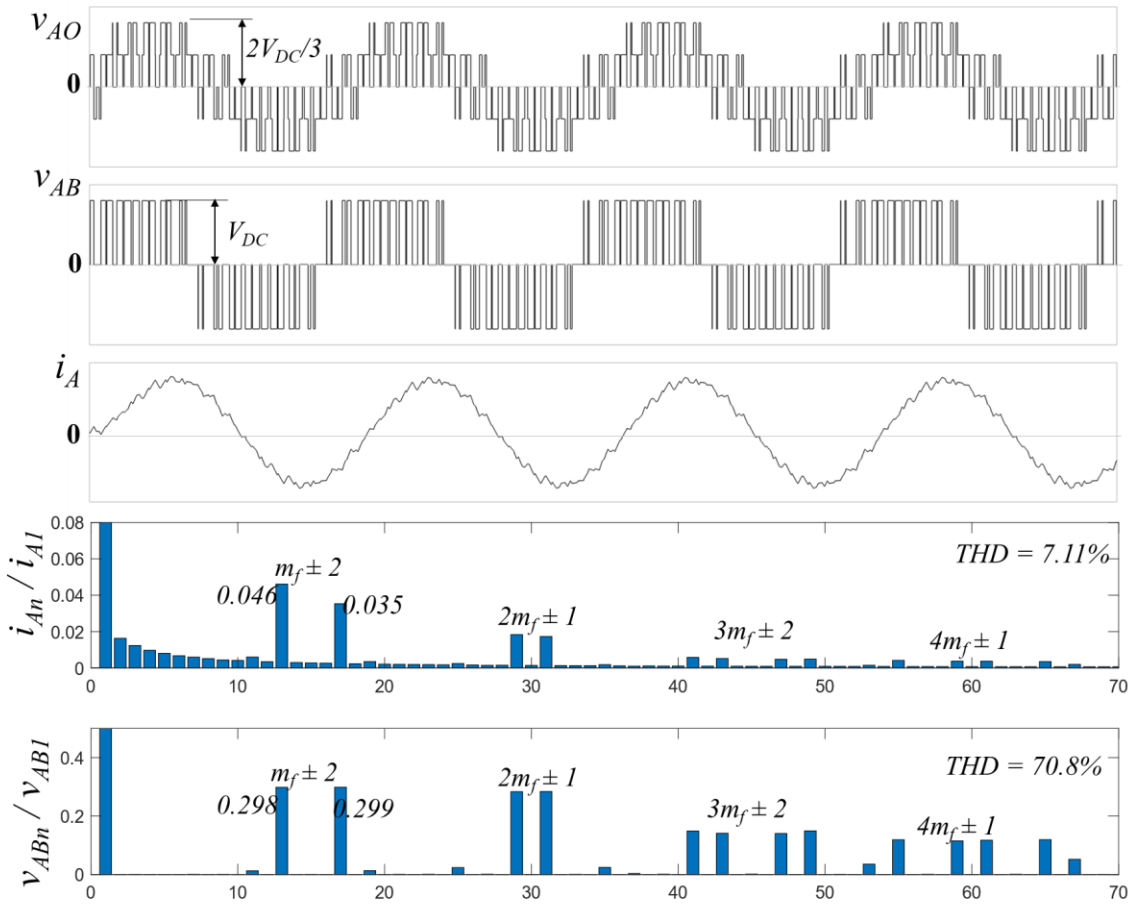


Figure 2.13. Simulated waveform of the two-level VSI operating at $f_m = 100Hz$, $m_a = 0.9, m_f = 15$, and $V_{DC} = 400V$. Load conditions are $L = 20mH$, and $R = 20\Omega$.

Due to the process of switching, both voltage and current wave have harmonic components, as demonstrated in Figure 2.3. These harmonic components are centered around m_f and its multiples, $2m_f$ and $3m_f$. The harmonics makes additional losses such as copper and iron losses in motor, and they amplify torque ripple. The effectiveness of this waveform can be articulated by the total harmonic distortion (THD), as expressed in Equation 2.4, where v_k and i_k are the harmonic components of the voltage and current, and v_1 and i_1 are the fundamental component of the voltage and current. A lower THD value signifies that the waveform is closer to the sinusoidal form, leading to improved control performance and superior motor efficiency.

$$THD_v = \frac{\sqrt{\sum_{k=2}^{n} v_k^2}}{v_1},\ THD_i = \frac{\sqrt{\sum_{k=2}^{n} i_k^2}}{v_1} \qquad \text{Equation 2.5}$$

The linear modulation range is defined for when the MI is less than or equal to 1, while overmodulation is defined for when MI exceeds 1. The root mean square (rms) value of the fundamental line-to-line voltage V_{LL1} can be calculated using Equation 2.5 and Equation 2.6.

$$V_{LL1} = 0.612 \times m_a \cdot V_{DC}, \text{ when } m_a \leq 1 \qquad \text{Equation 2.6}$$

$$V_{LL1} = 0.78 \times V_{DC}, \text{ when } m_a > 1 \qquad \text{Equation 2.7}$$

The maximum rms value of the line-to-line voltage are $0.612V_{DC}$ and $0.78V_{DC}$, respectively. Despite its simplicity, SPWM has the disadvantage of being limited to a maximum output voltage of 0.612. Space Vector PWM (SVPWM) allows for more voltage utilization.

SVWPM is one of the widely used for EV traction inverter. In the context of switching states for a three-phase inverter, the "P" denotes that the top switch is in the on-state in the phase leg, whereas "O" signifies that the bottom switch is on. As displayed in Table 2.1, there are eight possible switching states in total. In the PPP state, referring to the circuit in Table 2.1, the upper switches (S1, S3, and S5) of the A, B, and C phases, respectively, are turn-on. Consequently, the space vector, the resultant of the vector sum of these three vectors, amounts to zero. Similarly, for the OOO state, where the bottom switches are on, the vector sum is also zero. These two scenarios are hence referred to as zero vectors. The other remained six states are the active vectors that are 60^o out of phase with each other. These six active vectors form a hexagon in the space vector diagram, as seen in Figure 2.4. The hexagon that is generated from these six active vectors can be subdivided into a total of six sectors. Each sector corresponds to a unique combination of switch states, which in turn determines the output voltage vector of the inverter. The corresponding vector sums for each active states are presented in Table 2.1. These active vectors play a significant role in determining the inverter's output voltage and thus the performance and efficiency of the overall drive system.

Table 2.1. Space vector and on-state switch on 8 switching state of SVPWM.

Space Vector		Switching State	On-state Switch	Vector Definition
Zero Vector	$\overrightarrow{V_0}$	PPP	S1, S3, S5	0
		OOO	S2, S4, S6	$\frac{2}{3}V_{DC}e^{j0}$
Active Vector	$\overrightarrow{V_1}$	POO	S1, S4, S6	$\frac{2}{3}V_{DC}e^{j\frac{\pi}{3}}$
	$\overrightarrow{V_2}$	PPO	S1, S3, S6	$\frac{2}{3}V_{DC}e^{j\frac{\pi}{3}}$
	$\overrightarrow{V_3}$	OPO	S2, S3, S6	$\frac{2}{3}V_{DC}e^{j\frac{2\pi}{3}}$
	$\overrightarrow{V_4}$	OPPP	S2, S3, S5	$\frac{2}{3}V_{DC}e^{j\frac{3\pi}{3}}$
	$\overrightarrow{V_5}$	OOP	S2, S4, S5	$\frac{2}{3}V_{DC}e^{j\frac{4\pi}{3}}$
	$\overrightarrow{V_6}$	POP	S1, S4, S5	$\frac{2}{3}V_{DC}e^{j\frac{5\pi}{3}}$

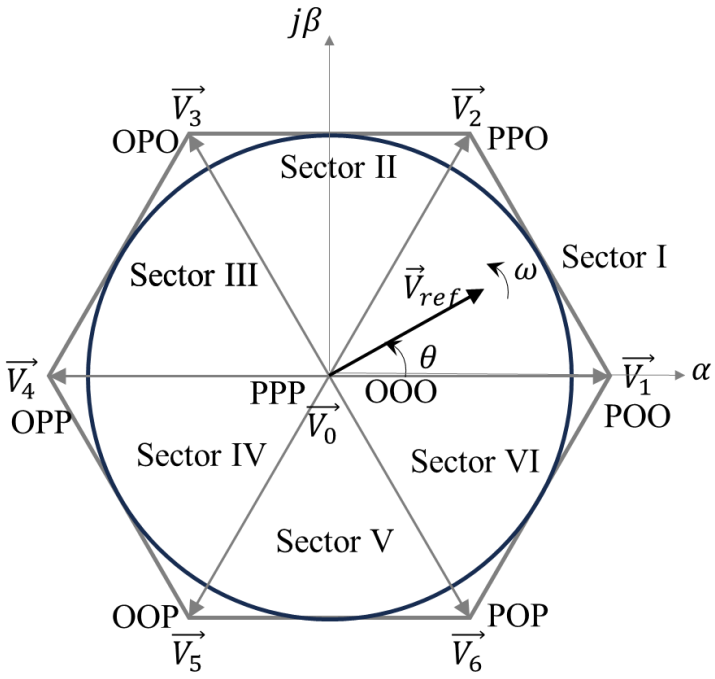


Figure 2.14. Space vector diagram of a two-level VSI

The conception of this activation vector originates from Clarke's Transformation, which transforms the three-phase phase voltage, as demonstrated in Equation 2.7, into a stationary reference frame [20]. Clarke's Transformation, or α-β transformation, is a mathematical technique employed in the analysis and control of three-phase systems. This transformation simplifies the mathematical complexity involved in the analysis of three-phase systems, making it easier to visualize and control these systems.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_{AO} \\ v_{BO} \\ v_{CO} \end{bmatrix} \quad \text{Equation 2.8}$$

v_α and v_β are the two-phase voltages in the α-β plane. From these, the space vector can be expressed as Equation 2.10 by combined Equation 2.7, 2.8, and 2.9. Each space vector obtained from these in shown in Table 2.1.

$$\vec{V} = v_\alpha + jv_\beta \quad \text{Equation 2.9}$$

$$e^{jx} = \cos x + j \sin x \quad \text{Equation 2.10}$$

$$\vec{V} = \frac{2}{3}\left[v_{AO}e^{j0} + v_{BO}e^{j2\pi/3} + v_{CO}e^{j2\pi/3}\right] \quad \text{Equation 2.11}$$

In Figure 2.4, the reference voltage $\vec{V}_{ref}$ to be controlled rotates at a speed ω. Essentially, what this implies is that a reference voltage, with a magnitude defined by the length of $\vec{V}_{ref}$ and a specified speed ω, can be synthesized by the suitable combination of active vectors available in this space vector diagram for each switching state. The dwell time for the stationary active vectors represents the duty-cycle of the chosen switches during a sampling period T_s. $\vec{V}_{ref}$ can be synthesized as a combination of one zero vector and two adjacent vectors in the space vector plane. The dwell time of each vector can be accurately calculated using the relationship expressed in Equations 2.11 and 2.12, where T_a, T_b, and T_0 are the dwell time for the vector $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_0$, respectively.

$$\vec{V}_{ref}T_s = \vec{V}_1T_a + \vec{V}_2T_b + \vec{V}_0T_0 \quad \text{Equation 2.12}$$

$$T_s = T_a + T_b + T_0 \quad \text{Equation 2.13}$$

The dwell time when $\vec{V}_{ref}$ is at Sector I can be expressed by Equation 2.13, and shown in Figure 2.5.

$$T_a = \frac{\sqrt{3}T_sV_{ref}}{V_{DC}}\sin\left(\frac{\pi}{3} - \theta\right)$$

$$T_b = \frac{\sqrt{3}T_sV_{ref}}{V_{DC}}\sin(\theta) \quad \text{Equation 2.14}$$

$$T_0 = T_s - T_a - T_b$$

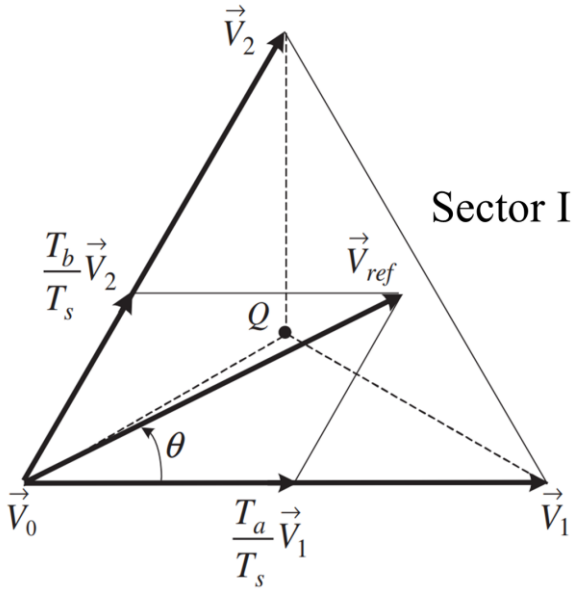


Figure 2.15. The reference voltage $\vec{V}_{ref}$ synthesized by $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_0$ when $\vec{V}_{ref}$ is at Sector I.

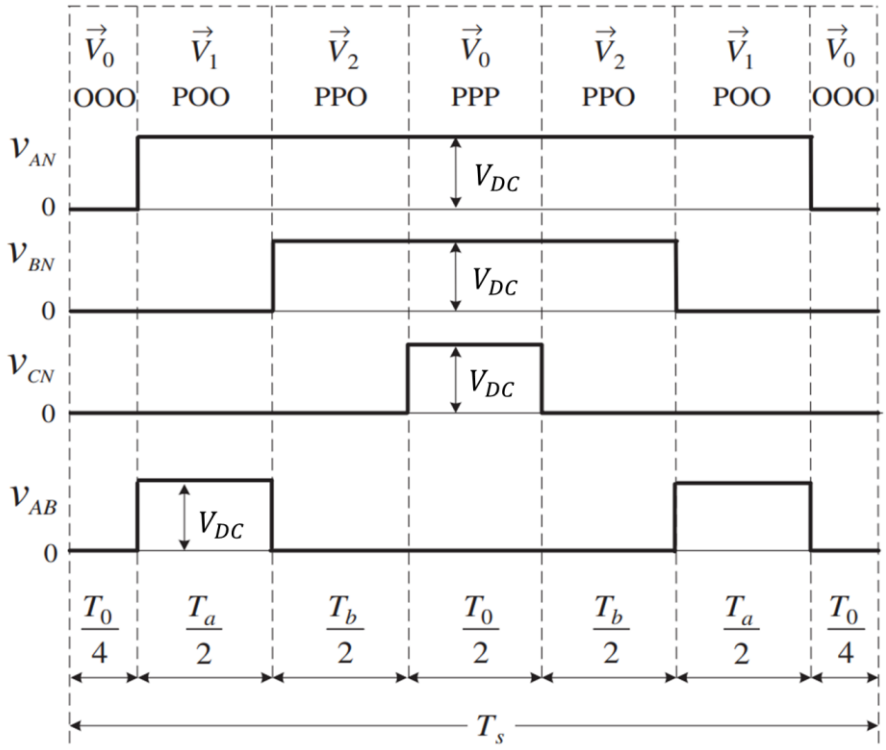


Figure 2.16. Typical seven-segment switching sequence for $\vec{V}_{ref}$ in Sector I.

The switching sequence shall be designed to minimize the number of switching during sampling period. Figure 2.6 presents the typical switching sequence with seven-

segment in Sector I. Figure 2.6 illustrates the switching sequence for Sector 1, composed of a standard seven-segment pattern. By powering the three-phase switches on and off in this designated order, a reference voltage can be generated with the fewest possible number of switching operations. The order of switching for other sectors should also follow a sequence that leads to the minimum number of switching per period. This minimization of switching events contributes to a decrease in switching losses, thereby improving the overall efficiency of the system.

As depicted in Figure 2.4, the maximum controllable voltage using SVPWM is equal to the radius of the inscribed circle within the hexagon. At this maximum, the rms value of the line-to-line voltage is $0.707V_{DC}$. Hence, SVPWM, while being a more complex control scheme compared to others, enables a higher voltage utilization. This contributes to improved power quality and efficiency, justifying its implementation despite the complexity.

2.1.2 Comparison of Multi-level Inverter Topology

As described in previous chapter, the most common type of inverter topology used in EVs is the two-level inverter. However, multi-level inverter topologies have gained increasing attention in recent years due to their potential benefits. Research has been conducted on various types of multi-level inverters due to their advantages such as high efficiency, high power density, better output waveform quality, low dv/dt and EMI, and inherent fault-tolerance [21-25]. This is particularly significant in high-voltage and high-power applications. Recently, high-voltage electric drive systems like 800V systems have gained attention, making multi-level inverter topologies a fresh alternative in this field. Compared to the traditional 400V system, the 800V system offers benefits such as faster battery charging speed, high efficiency due to lower motor current, which in turn reduces copper loss, and a decrease in cable thickness [26]. However, the high voltage can lead to a high dv/dt, impacting not only the power device of the inverter but also the insulation characteristics of the motor, potentially affecting reliability. A multi-level inverter can serve as an effective solution to this problem. The most common types of multi-level

inverters are the diode-clamped, flying capacitor (FC), and cascaded H-bridge (CHB) inverters.

The diode-clamped inverter, also known as a neutral-point-clamped (NPC) inverter which was introduced by Nabae et al. [27], uses diodes to clamp the DC link voltage to achieve different voltage levels. This inverter was modelled to produce a small harmonic output voltage for a high efficiency motor drive. Figure 2.7 presented a three-level NPC topology. The additional neutral point of the converter allows the three states of the voltage level $V_{DC}/2$, $-V_{DC}/2$, and *0*. For $V_{DC}/2$, S1and S2 should be turned on, while S3 and S4 are turned on for $-V_{DC}/2$. And for *0* state, S2 and S3 should be turned on.

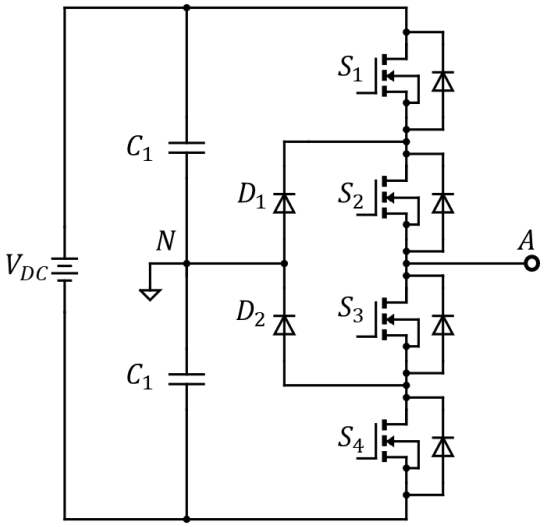


Figure 2.17. Three-level NPC inverter topology

In comparison with other multilevel topologies, NPC inverter has been widely used due to high efficiency and simplicity [28-30]. This system utilizes a common DC-link, which offers the benefit of compactness by minimizing the number of capacitors required. However, if precise monitoring and control mechanisms are not in place, several drawbacks may arise. These include the risk of overcharging and discharging of the DC voltage, as well as uneven distribution of losses among the switches. To mitigate these issues, it is crucial to implement accurate monitoring and complex control techniques within the system [31].

The FC inverter uses capacitors instead of the clamping diodes to divide the DC link voltage into different levels [32]. The three-level FC inverter topology is presented in Figure 2.8. In the design of this topology, it's typical that one would need (*n-1*) capacitors for *n* distinct output voltage levels and (*n-1*) × (*n-2*)*/2* flying capacitors are needed. These capacitors are arranged in a ladder-like configuration, with each subsequent capacitor possessing a different voltage than its neighboring capacitor. In the case of FC switching technology, the switching mechanism is comparable to that of a NPC inverter, with a slight variation in the 0 state [33]. For the 0 level, either S1, S3 or S2, S4 is turned on. A notable advantage of this topology is that it provides redundancies for inner voltage levels. This means that multiple valid switching combinations can produce the desired output voltage. Furthermore, the redundancy of clamped capacitors in each phase helps maintain balanced capacitor voltages, a feature that has been validated in numerous studies [34]-[36]. However, a major drawback to this topology lies in its requirement for a large number of capacitors. This requirement results in significant space implications, which negatively affect the power density of the inverter.

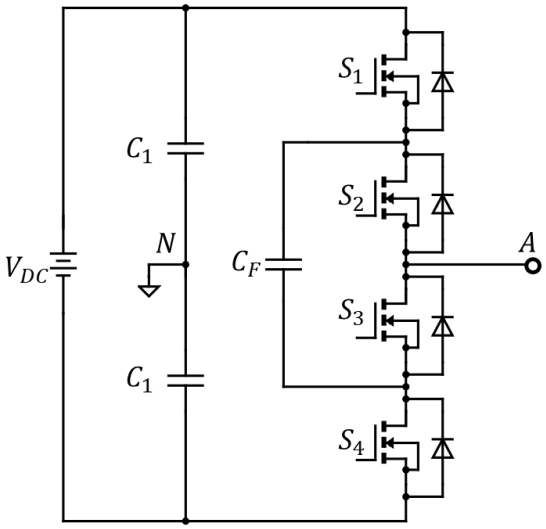


Figure 2.18. Three-level FC inverter topology.

Figure 2.9 shows the CHB inverter topology. This inverter consists of a series of H-bridge cells, each connected to a separate DC source, which provides different voltage levels [37]. When one H-bridge is connected, it has a three voltage levels. For producing

$+V_{DC}$ and $-V_{DC}$, switches S1 and S4, and S2 and S3 are activated respectively. On the other hand, the output voltage can be obtained by enabling either the S1 and S2 or the S3 and S4 switch pair. This topology enhances the number of voltage steps in the output voltage to (*2n+1*), where *n* denotes the total number of separate DC power supply units. Thus, for applications demanding distinct DC power sources, CHB inverters represent a beneficial solution. Furthermore, studies have examined the use of the CHB topology to control battery voltage as an alternative to a Battery Management System (BMS) [38,39]. However, in the context of general EVs, it proves challenging to derive separate connections from each cell within a battery pack. This presents a significant hurdle to the broad implementation of this approach.

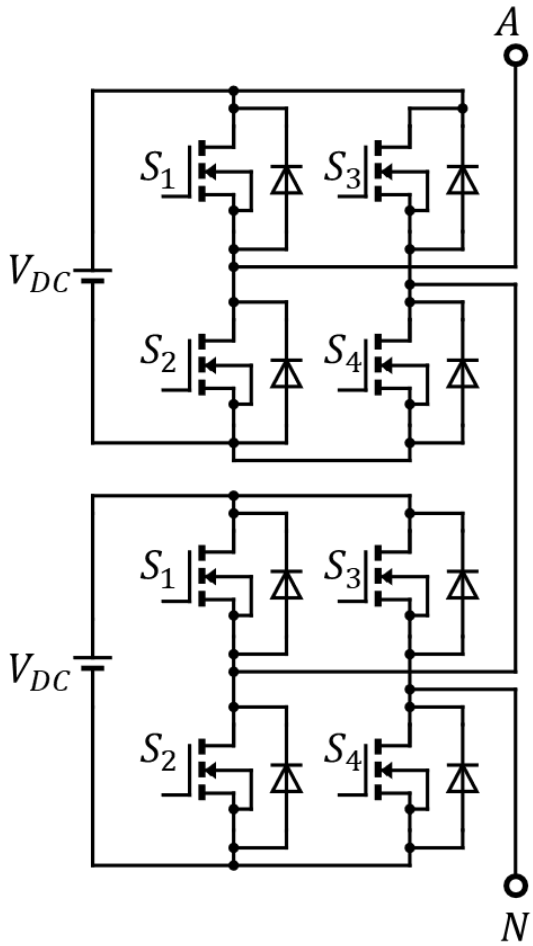


Figure 2.19. Five-level CHB inverter topology.

The Active NPC inverter is a one of the half-brige neutral point clamped inverter family and it was proposed in [40] as an alternative to NPC inverter, with the aim of

improving loss balancing and better utilization of semiconductor device areas in the inverter. This advancement was achieved by replacing diodes in NPC inverters with active switches, which allowed for the creation of additional zero states. Furthermore, this replacement allowed for different modulation strategies to be applied with flexible utilization of redundant switching states. Details of this research for ANPC are covered in depth in the next chapter.

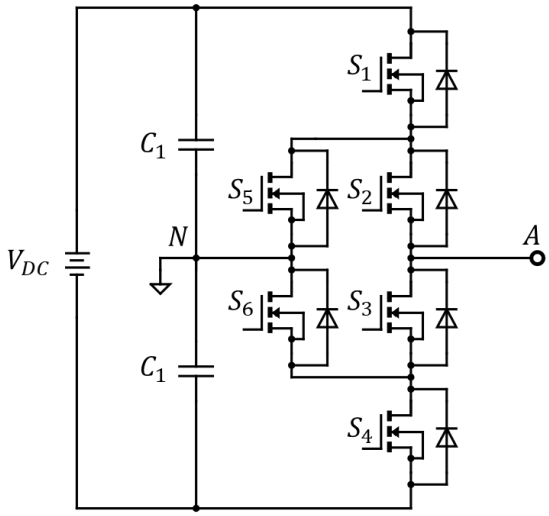
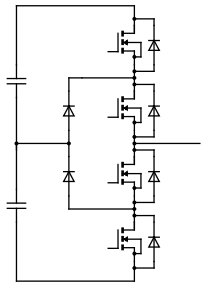
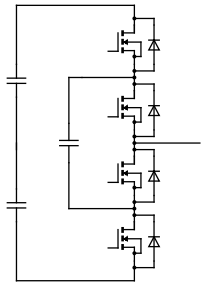
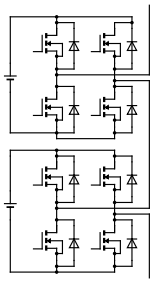
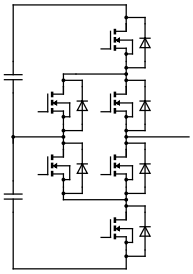


Figure 2.20. Three-level ANPC inverter topology.

In Table 2.2, a comparison of the advantages and disadvantages of prevalent multi-level inverter topologies is presented. The ANPC presents a more complex control strategy than the NPC, but it offers the possibility of choosing an approach best suited to the application with a range of switching techniques, and it allows for balancing losses among power devices. The FC topology, on the other hand, has size constraints due to the need for a capacitor, a disadvantage in the context of electric drive inverters that require compactness. As previously mentioned, the CHB needs a separate voltage source. Efficiency comparisons across each topology, as demonstrated in [41], highlight ANPC as the most efficient. In, [42] further shows a reduction in energy loss when using 3-level and 5-level ANPC compared to a 2-level system. In this study, A discussion will revolve around different PWM strategies and their benefits in traction inverter for EVs, with particular emphasis on three-level ANPC inverter.

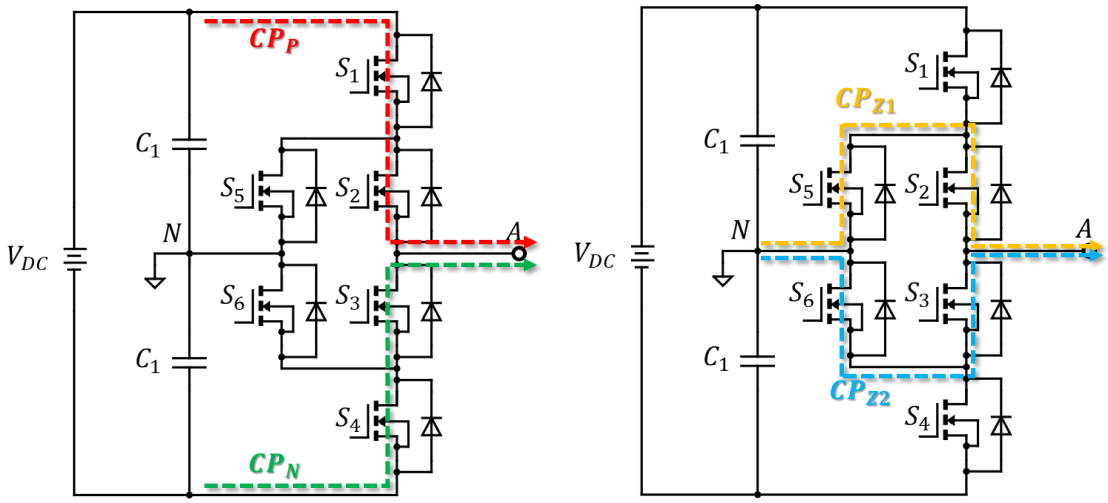
Table 2.2. Comparison of multi-level inverter topologies.

Topology	Schematics	Advantages	Disadvantages
NPC		• No floating capacitors • Good dynamic response • Simple design • Low cost and compact in 3-level	• Increased cost and reduced reliability with high level • Loss unbalancing
FC		• Cost efficient in high level	• High no. of flying capacitors • Complex control • High stored energy in capacitors • Large volume • Low reliability
CHB		• High reliability • Simple control • No floating capacitors • Module design	• Require isolated DC sources
ANPC		• No floating capacitors in 3-level • Good dynamic response • Simple design • Loss balancing • Low cost and compact in 3-level	• Increased floating capacitors with high-level • More power switch in 3-level • Different voltage rating of power switches with high-level

2.1.3 Three-Level Active Neutral Point Clamped Inverter

As can be seen in Figure 2.10, the ANPC inverter is formed by six active power switches S1-S6 to achieve a three-level output voltage, and the voltage rating of each power devices have a half of the DC-link voltage. Compared to NPC inverter, various zero output voltage state can be implemented for active loss balancing. Studies have been conducted

on the application of ANPC inverters in diverse sectors such as photovoltaic systems [43,44] and EV charging [45] as well as traction applications [42,46]. An examination and comparison of the efficiency and output of various strategies for ANPC have been conducted [45,47,48]. The aim is to achieve a balanced distribution of switching losses or to double the effective switching frequency at the output. Figure 2.11 shows the main current paths of the three-level ANPC for P, N, and 0 state. As illustrated in (a), for the P state, current flows through the path CP_P and the current in the reverse direction behaves identically, and the output voltage v_{AN} is $+V_{DC}/2$. Similarly, for the N state, a current flow through CP_N and exhibits an output voltage value of $-V_{DC}/2$. In this topology, there are two current paths for the zero state, CP_{Z1} and CP_{Z2}. This combination paves the way for a multitude of PWM strategies. Consequently, the loss distribution or output value for each switch diverges slightly based on the adopted strategy.



(a) (b)

Figure 2.21. Three-level ANPC inverter topology and current paths (a) P and N state (b) 0 state

In [47], switching sequence for the PWM1 strategy is shown in Table 2.3. In this PWM1, the zero state current flows through a path CP_{Z1} for positive half cycle and CP_{Z2} for negative cycle. It has a relatively short commutation loop in transition between 0 state and P or N.

Table 2.3. Switching sequence and output voltage for PWM1 strategy

State	Switch						Current path	Output voltage
	S1	S2	S3	S4	S5	S6		
P	1	1	0	0	0	0	CP_P	$+V_{DC}/2$
O+	0	1	0	0	1	0	CP_{Z1}	0
O-	0	0	1	0	0	1	CP_{Z2}	0
N	0	0	1	1	0	0	CP_N	$-V_{DC}/2$

Table 2.4 shows the switching sequence for the PWM2 strategy in [47]. Compared to PWM1, it has a longer loop for the commutation.

Table 2.4. Switching sequence and output voltage for PWM2 strategy

State	Switch						Current path	Output voltage
	S1	S2	S3	S4	S5	S6		
P	1	1	0	0	0	1	CP_P	$+V_{DC}/2$
O+	1	0	1	0	0	1	CP_{Z2}	0
O-	0	1	0	1	1	0	CP_{Z1}	0
N	0	0	1	1	1	0	CP_N	$-V_{DC}/2$

In [48], loss balancing optimized PWM strategy is proposed. As can be seen in Table 2.5, during the 0 state, the current path is divided into two parallel paths CP_{Z1} and CP_{Z2}. In this case, there is only one 0 state, which makes implementation comparatively straightforward.

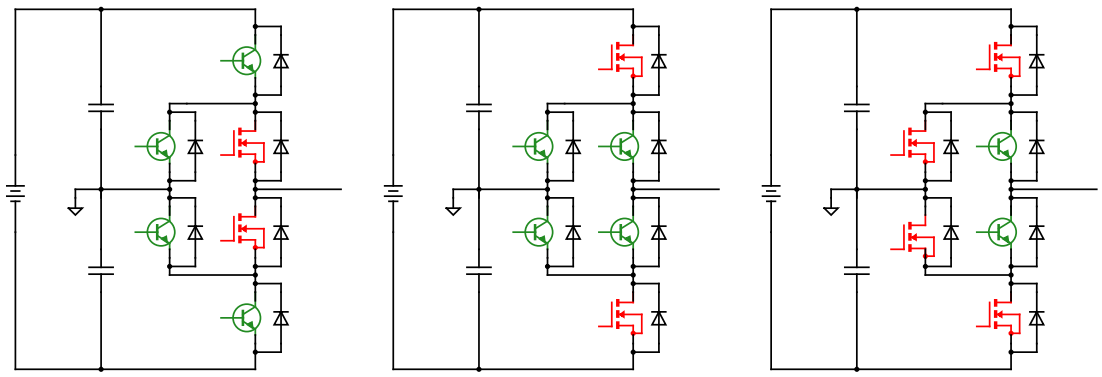
Table 2.5. Switching sequence and output voltage for PWM3 strategy

State	Switch						Current path	Output voltage
	S1	S2	S3	S4	S5	S6		
P	1	1	0	0	0	1	CP_P	$+V_{DC}/2$
O	0	1	1	0	1	1	CP_{Z1}& CP_{Z2}	0
N	0	0	1	1	1	0	CP_N	$-V_{DC}/2$

Moreover, several other PWM strategies have been studied. In [49], a PWM strategy, named Doubly Frequency PWM (DF-PWM), that incorporates four zero-states has been proposed, which is a combination of the aforementioned PWM1 and PWM2 strategies. The Splitting Switching Loss Distribution PWM (SSLD-PWM) method is also

introduced aiming for a more even loss distribution under a condition of a single power factor (PF) in [47].

The characteristics of PWM1 and PWM2 have been employed to propose a hybrid topology of Si and SiC. Figure 2.12 presents various hybrid three-level ANPC topologies that integrate Si and SiC power devices. As will be discussed in a later chapter, SiC has less switching loss than Si. Thus, for devices that switch frequently as per a PWM strategy, substituting with SiC can lead to lower losses. In [50], the merits of the full-SiC topology using the PWM2 strategy and the topology of Figure 2.12 (a) were investigated. In [51], losses and thermal performance of the same 4Si-2SiC hybrid1 topology were analyzed according to various PWM strategies. Furthermore, [52] compared and analyzed the topologies (a) and (b), and [53] studied a comprehensive hybrid topology. A PWM method was proposed for the topology that comprised by different parallel devices from Si and SiC in the same switch leg [54].

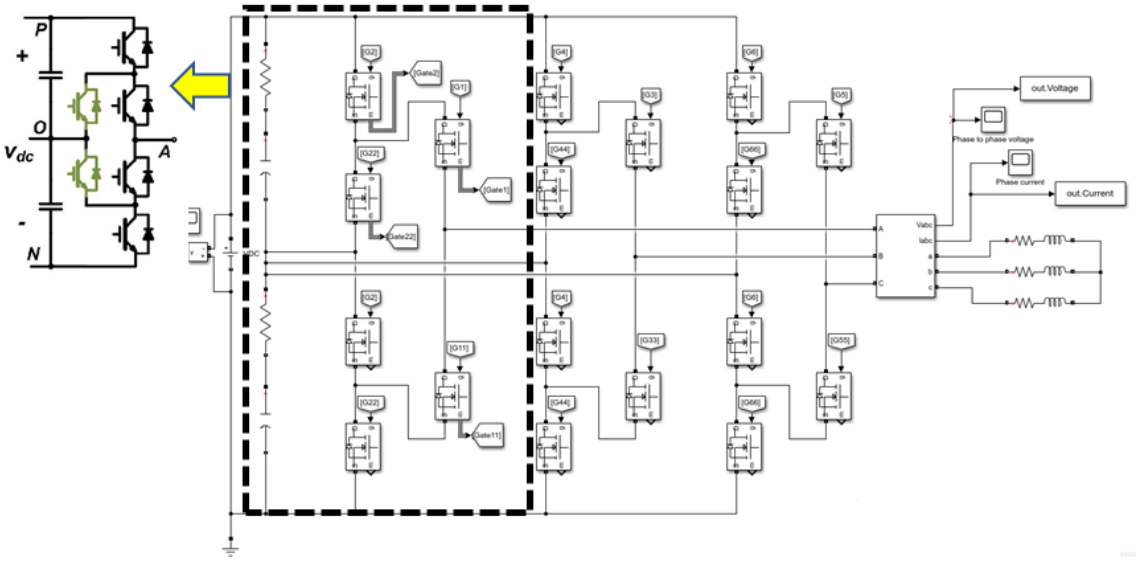


(a) (b) (c)

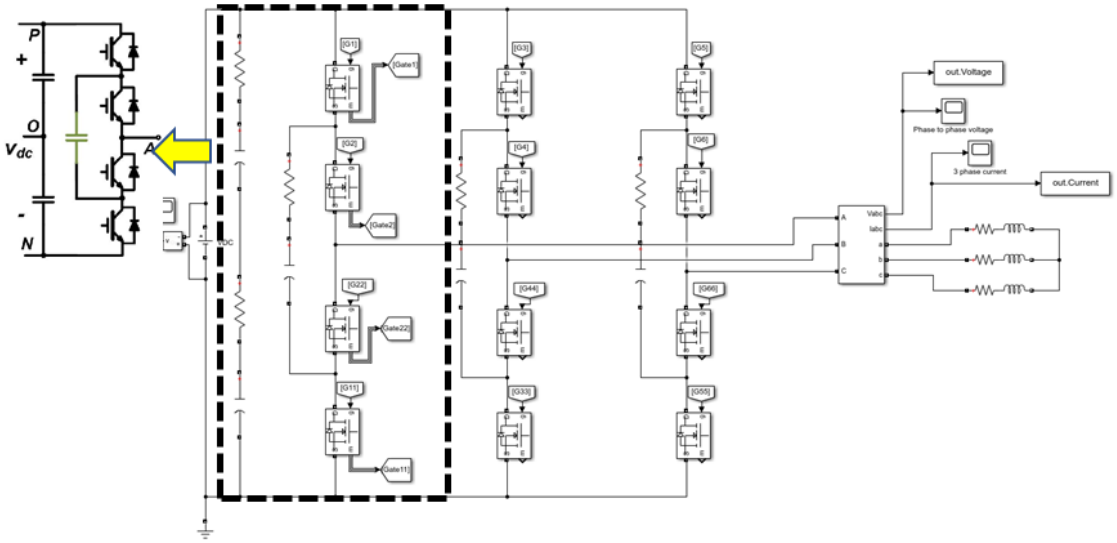
Figure 2.22. Different hybrid three-level ANPC topology (a) 4Si-2SiC hybrid1 (b) 4Si-2SiC hybrid2 (c) 2Si-4SiC hybrid

2.1.4 Effect of Multi-level Inverter Topology

In this chapter, the topologies of a 2L inverter, 3L-ANPC, and a 3L-FC inverter are compared through a basic simulation, with an analysis conducted on the effects of multi-level elements. Both a three-phase, three-level FC inverter and an ANPC inverter have been modeled through MATLAB SIMULINK as displayed in Figure 2.13. The voltage and current waveforms are examined utilizing a carrier-based PWM strategy.



(a)



(b)

Figure 2.23. MATLAB SIMULINK simulation for (a) 3L-ANPC (b) 3L-FC

As demonstrated in the results presented in Figure 2.14, it's evident that the voltage level of the output line-to-line voltage increases compared to the 2-level system, creating a cascading pattern and approximating a sine wave. Figure 2.15 illustrates the current waveform for each topology along with the harmonic analysis of the waveform under an R-L load state. At the same switching frequency, the 3-level topology can generate a current waveform that is closer to a sine wave compared to the 2-level system. This is also reflected in the THD, which is considerably reduced from 4.4% to 2.3%. Consequently,

this reduction in THD decreases iron loss and AC copper loss in the motor, which in turn enhances the overall system efficiency.

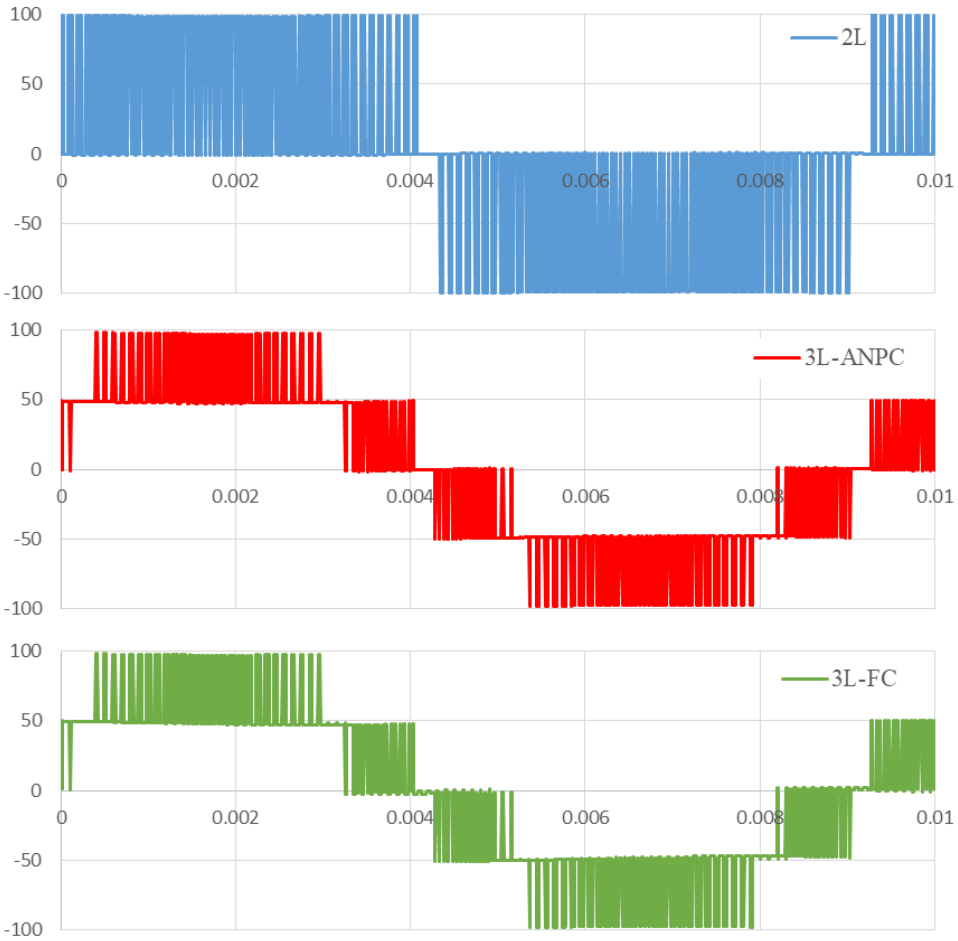
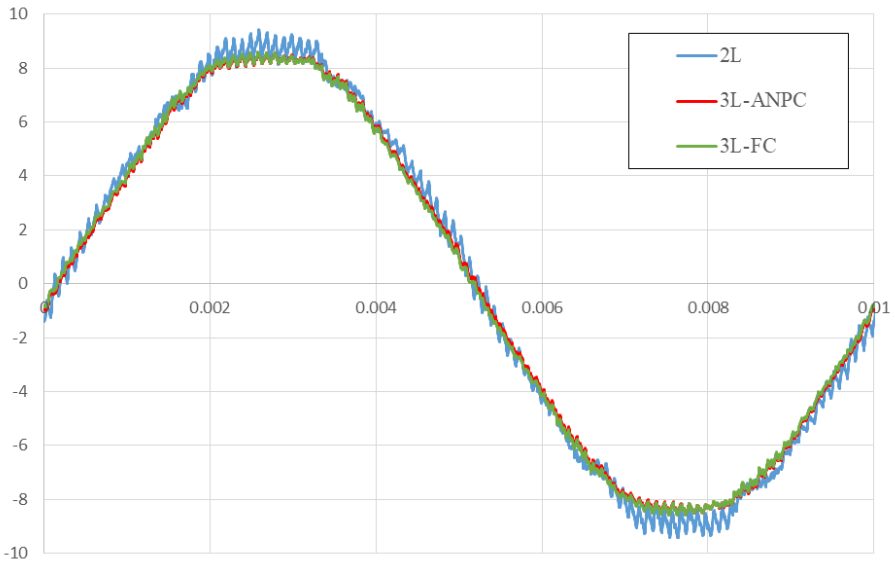
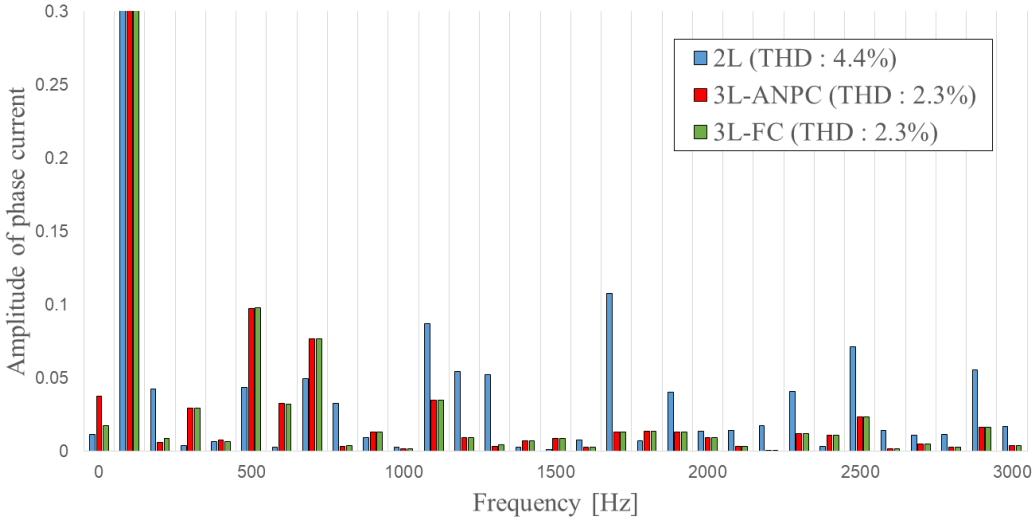


Figure 2.24. Comparison of output line-to-line voltage with 2L, 3L-ANPC and 3L-FC



(a)



(b)

Figure 2.25. Comparison of (a) output current (b) harmonics of output current with 2L, 3L-ANPC and 3L-FC

2.2 Wide-band Gap Devices

Numerous research endeavors focus on traction inverters to bolster the energy efficiency of electric vehicles [55-58]. Particularly active is the research on power semiconductor devices, which are significant contributors to power loss associated with high current conduction and switching. The efficiency of the power converter system, inclusive of the traction inverter, is substantially contingent on the selection of

semiconductor devices and the switching frequency. Attributable to decades of improvements in fabrication and optimization, an abundant supply of materials, vast manufacturing facilities, and an unrivaled low cost, Si maintains its position as the most utilized material for the fabrication of power semiconductor devices. This is largely due to the availability of the technology and the accessibility of the materials [59]. Currently, Si based IGBT devices are prevalently employed in traction systems for electric drives due to their capacity for high current values. However, their intrinsic physical limitations pose a hurdle to achieving enhanced performance. Concurrent with the swift progression of semiconductor technology, WBG power semiconductor devices, predicated on SiC and GaN, have emerged as the forthcoming generation of power semiconductor devices [60-64]. The use of WBG devices has clear advantages when it comes to improving the efficiency of inverters and reducing filter size under high voltage conditions. This is due to their impressive breakdown voltage and lower switching losses compared to Si-based devices. Additionally, increasing the switching frequency can lead to a decrease in THD in output voltage and current, which greatly contributes to optimizing motor efficiency. In [61], the utilization of WBG materials in place of Si in EV motor drive facilitates an enhancement in efficiency by 1.4-4.4% and a total mass reduction by 46%. The first WBG power devices to attain the pinnacle of technology readiness levels encompass n-type SiC power MOSFETs, SiC-based Schottky Barrier Diodes (SBDs), and GaN High Electron Mobility Transistors (HEMTs) [62]. These devices, designed specifically for power electronics applications, have been in large-scale production for several years. Concerted efforts to integrate these advancements into vehicular applications are already in progress. Tesla is a pioneer in this sector, becoming the first EV manufacturer to fully adopt SiC technology. Furthermore, Toyota has conducted on-road tests of SiC devices, including transistors and diodes, in inverters and internal DC-DC converters for their Camry Hybrid prototypes. Contemporary auto manufacturers are incorporating WBG devices, including the SiC-MOSFETs, into their EV applications.

2.2.1 WBG Material Properties

The electrical performance of a semiconductor device is fundamentally intertwined with the physical properties inherent to the specific material. Electrons in solid materials occupy varying energy bands surrounding an atom. The highest energy band, along with the immediately inferior one, are termed the conduction band and valence band, respectively. Current conduction in a material arises from the movement of electrons in the conduction band from one atom to another. The displacement of an electron yields a hole in the valence band of the atom, imbuing it with a positive charge. These holes can also move in the materials in the opposite direction of electrons and contribute to current conduction. Figure 2.16 offers a representation of the energy bands characteristic of metals, semiconductors, and insulators. In semiconductors and insulators, these valence and conduction bands are separated by an energy band gap E_g. On the other hand, in the case of metal, E_g is very small, or the two bands are overlapped, that means E_g does not exist. This band gap symbolizes the energy requisite for transitioning an electron from the valence band to the conduction band, or conversely. WBG materials exhibit an energy bandgap (2-4eV) superior to that of traditional silicon (1-1.5eV).

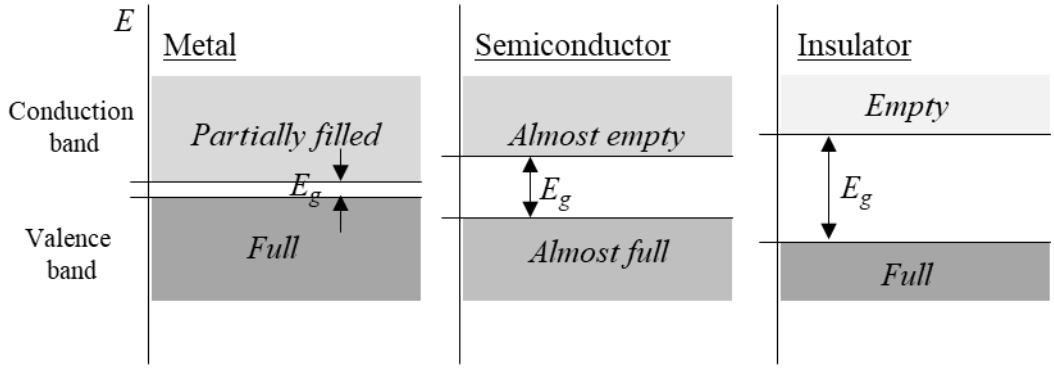


Figure 2.26. Energy band diagram of solid metal, semiconductor, and insulator.

Critical material properties of prevalent WBG substances like 4H-SiC polytype SiC, GaN, diamond, and Si are exhibited in Table 2.6. It is evident that the bandgaps of SiC, GaN, and diamond surpass that of Si by approximately three to five times. This signifies the necessity of elevated energy temperature to dissociate a bond of electron and facilitate

its transition between bands. The intrinsic carrier concentration[1], n_i is characteristically lower in WBG materials compared to Si, owing to the elevated energy bandgap E_g. The value of n_i depends exponentially on E_g and temperature like Equation 2.14, WBG can function at considerably higher temperatures with the same leakage current at Si devices, or at the same temperature with significantly reduced leakage current.

Table 2.6. Comparison of WBG materials properties with Si, according to [65-67].

Property	**Si**	**4H-SiC**	**GaN**	**Diamond**
Bandgap, E_g [eV]	1.1	3.2	3.4	5.45
Dielectric constant, ε_r	11.8	10	8.9	5.5
Critical electric field, E_{crit} [MV/cm]	0.3	2.0	3.3	5.6
Thermal conductivity, κ [W/cm-K]	1.5	4.5	2.4	20
Electron mobility, μ_n [cm2/V-s]	1,350	720	1,300	1,900
Saturated electron velocity, v_{sat} [$\times 10^7$cm/s]	1.0	2.0	2.7	2.7
Baliga's Figure of Merit [BFoM]	1	500	2,400	9,000

$$n_i^2(T_j) = C \cdot T_j^3 \cdot e^{-\frac{E_g(T_j)}{k \cdot T_j}} \qquad \text{Equation 2.15}$$

Here, C is the coefficient related to a specific semiconductor, T_j is the junction temperature of the device, and k denotes Boltzmann's constant.

WBG materials also results in an extensive critical electric field E_{crit}, exhibiting a value that is 7 to 10 times that of Si. Such a value yields a significant blocking voltage, thereby facilitating high-voltage operations. For varying semiconductor materials, an increase in E_{crit} allows for the development of thinner devices at the same breakdown voltage. The breakdown voltage V_{BD} is proportional to the square of the critical electric field as illustrated in Equation 2.15, where ε_r is dielectric constant of semiconductor material, q is the elementary charge, n is the doping density.

$$V_{BD} \propto \frac{1}{2} \cdot \frac{\varepsilon_r}{qn} \cdot E_{crit}^2 \qquad \text{Equation 2.16}$$

[1] All power semiconductor device design relies on the assumption that doping levels are much higher than a material property called the intrinsic carrier concentration.

$$W_{drift} \propto \sqrt{\frac{2\varepsilon_r}{qn} V_{BD}} \qquad \text{Equation 2.17}$$

From Equation 2.16, for a given material, breakdown voltage and required device thickness depend inversely on doping. This implies that there is potential for increasing doping density or creating devices with thinner dimensions.

The resistance of the drift region r_{on} is defined as Equation 2.17, where μ_n is the electron mobility [68].

$$r_{on} = \frac{W_{drift}}{qn \cdot \mu_n} \qquad \text{Equation 2.18}$$

For a given voltage rating, employing higher doping levels allows for enhanced on-state performance due to reduced thickness. This in turn minimizes charge accumulation effects, leading to improved switching performance of the WBG devices. Additionally, the higher saturation velocity v_{sat} contributes to improved switching and augments the power capacity of these devices.

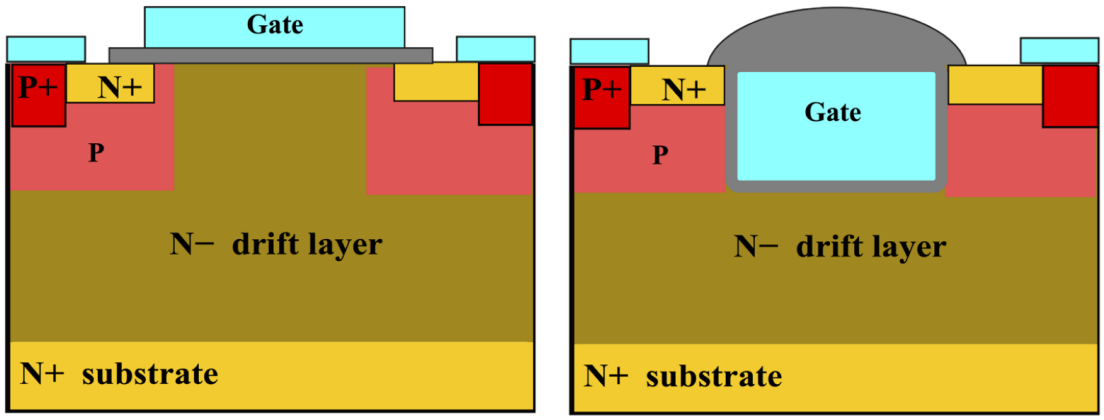
Based on the Equation 2.18 in [69], Baliga's figure of merit (BFoM) is presented in Table 2.6. This provides the insight into the conduction losses relative to the material properties in unipolar devices. As seen in Table 2.6, the BFoM for WBG materials is considerably higher than that of Si. This implies that, if BFoM is considered for material comparison, the on-state resistance of a unipolar device, based on GaN and SiC, can be reduced by a factor of 2400 and 500 respectively, as compared to a Si-based unipolar device operating at the same breakdown voltage. Diamond has a band gap of 5.45eV that is significantly larger than that of GaN and SiC, so it is categorized as Ultra-WBG device. Despite its superior characteristics, it isn't as broadly utilized as SiC and GaN due to cost-related concerns.

2.2.2 SiC MOSFET

One of the widely used the state-of-the-art WBG power devices is SiC MOSFET.

Power MOSFETs are unipolar voltage-controlled devices that manipulate voltage via the gate terminal and are configured in both npn and pnp structures. This alternating structure allows for the creation of two types of MOSFETs: enhancement npn and depletion

pnp mode MOSFETs. The enhancement mode MOSFETs employ the p-type layer as the device's channel, following a npn configuration. Conversely, depletion mode MOSFETs use the n-type layer as a channel in a pnp structure. Enhancement mode devices are typically off and use electrons as the majority carriers. Depletion mode devices, however, are usually on, utilizing holes as the majority carriers. Due to safety and controllability concerns, power electronics tend to favor enhancement mode MOSFETs over depletion mode ones, given that electrons possess nearly thrice the mobility compared to holes, and devices that are always off are typically preferred. Prominent structures of n-channel SiC-MOSFETs encompass a planar structure and trench structure, as depicted in Figure 2.17.



(a) (b)

Figure 2.27. The structure of (a) Planar SiC-MOSFET (b) Trench SiC-MOSFET, from [60].

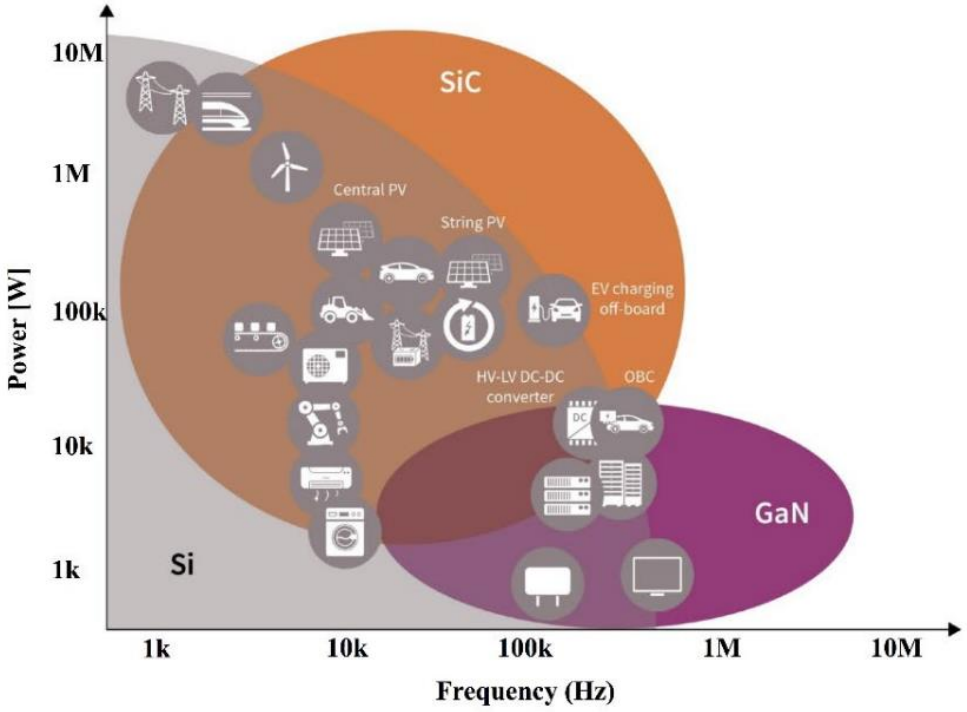
The planar SiC-MOSFETs, often considered the original structure, are simpler in design and easier to manufacture. The channel formation in these transistors occurs horizontally, and the gate oxide is only on the top surface of the channel. This results in a device with lower gate charge, making it suitable for high-frequency applications [70]. The planar structure's primary advantage lies in its robustness and reliability. The top-side gate oxide is less prone to electric field-related stresses because the field is less concentrated compared to trench structures. This property also contributes to better oxide reliability. However, planar SiC-MOSFETs generally have a higher on-resistance compared to trench SiC-MOSFETs. This is due to the lower channel density that results from the horizontal orientation of the channels. In terms of on-resistance, trench SiC-MOSFETs typically

outperform their planar counterparts due to higher channel density. This makes them suitable for applications where low on-resistance is critical. However, the added complexity in their manufacturing can increase the overall cost of these devices.

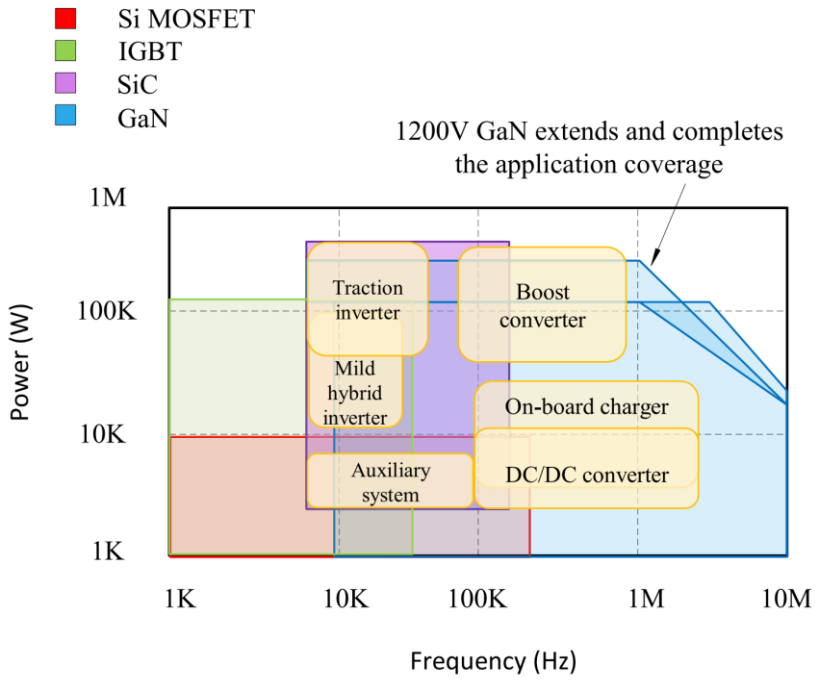
While the maximum junction temperature of a typical silicon-based device is around 150°C, SiC-MOSFETs can comfortably operate at temperatures up to 200°C and beyond, significantly enhancing their application potential. Furthermore, SiC-MOSFETs offer the possibility of high-frequency operation. Due to their lower switching losses compared to their silicon counterparts, SiC-MOSFETs allow the design of power converters that can operate at higher frequencies. Another key advantage of SiC-MOSFETs is their high voltage handling capability. SiC-MOSFETs have demonstrated their ability to handle high voltage levels, often up to several kilovolts. With low on-resistance, SiC-MOSFETs can replace the area occupied by Si-IGBTs in conventional EVs [71].

2.2.3 Comparison Si vs SiC, GaN

There is a significant difference between GaN and SiC when it comes to their electron mobility, as shown in Table 2.6. This suggests that GaN may be more appropriate for high-frequency applications [72]. On the other hand, SiC exhibits greater thermal conductivity than GaN, theoretically implying that SiC devices can operate at higher power densities than their GaN counterparts. The intrinsic ability of SiC power devices to withstand high temperatures allows for improved thermal management and a decrease in the size of heat sinks and cooling systems. The ability to switch faster with fewer switching losses directly results in a reduction in the volume of passive components and heat sinks, thereby leading to higher power density. When high power is a critical feature of a device, SiC semiconductors have an edge over GaN. Moreover, SiC devices utilize fewer components and offer a wide bandgap with substantial electric field strength. This allows for the achievement of higher voltages with extremely low resistance per unit area, thereby extensively reducing power loss. A comparison of the main application areas for overall Si, SiC and GaN in terms of frequency and power rating is shown in Figure 2.18.



(a)



(b)

Figure 2.28. (a) Power-frequency plane of Si, SiC, and GaN for different application, from [60] (b) Power-frequency plane of Si-MOSFET, IGBT, SiC, and GaN for different EVs applications, from [73].

Compared to Si, SiC can operate in a higher frequency range, and can replace existing Si-IGBT with SIC-MOSFET with high power, and is particularly suitable for EV traction inverters. In the case of GaN, it is more suitable for the high frequency area, but it is true that it is still inferior to SiC in the voltage level and high-power area.

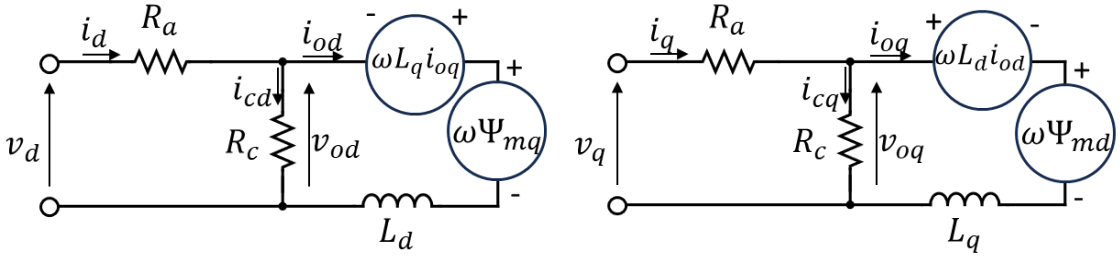
2.3 High-Speed, High-Power Density PMSM

In the context of EVs, electric machines require certain key performance characteristics to ensure the efficient operation of the vehicle. The critical features include high efficiency, high torque and power density, a wide operating range, high durability and reliability, and cost-effectiveness. High efficiency ensures the maximum conversion of electrical energy into mechanical energy, thereby extending the vehicle's range. A high torque and power density provide the vehicle with sufficient acceleration and top speed. Furthermore, the motor must operate effectively across various speeds and loads, ensuring optimal power delivery from a standstill to the vehicle's maximum speed. In terms of durability and reliability, the motor must endure harsh automotive conditions with minimal maintenance requirements over the vehicle's lifetime. Cost-effectiveness remains paramount to keep the EV accessible to consumers. Given these demands, Permanent Magnet Synchronous Motors (PMSM) have become a popular choice for EV traction applications, due to their numerous advantages [74-75]. PMSMs, using permanent magnets to generate a magnetic field, offer high efficiency and power density since no current is required in the rotor to create the magnetic field. Additionally, PMSMs typically possess superior thermal characteristics, crucial in EVs where motors often operate at high speeds and torques for extended periods. Another advantage lies in the high torque to inertia ratio, which ensures excellent dynamic performance, crucial for rapid acceleration and deceleration in EVs.

2.3.1 IPMSM

Neodymium magnets are commonly used in PMSM for traction motors due to their high magnetic strength [74]. Among the various types of PMSMs, Interior-mounted PMSMs (IPMSMs) are particularly favored. Unlike Surface-mounted PMSM (SPMSM),

IPMSMs can optimize the use of reluctance torque due to the unique characteristics of the rotor design, and they also have advantages in the flux-weakening area during high-speed operations [77]. Figure 2.19 illustrates the d-q axis equivalent circuit of an IPMSM, which is a valuable tool for analyzing and understanding the behavior of the motor in the rotating reference frame. This equivalent circuit model includes the impacts of both d-axis and q-axis parameters. The d,q transformation, also known as the Park transformation, is indeed an extremely beneficial mathematical tool in the field of motor control. It translates time-varying parameters, which depend on the rotation angle in a three-phase system, into steady DC components. This transformation greatly simplifies the analysis and control of AC motors [78].



(a) (b)

Figure 2.29. IPMSM equivalent circuit (a) d-axis (b) q-axis

Additionally, Figure 2.20 presents the phasor diagram of the IPMSM, featuring d-q axis components.

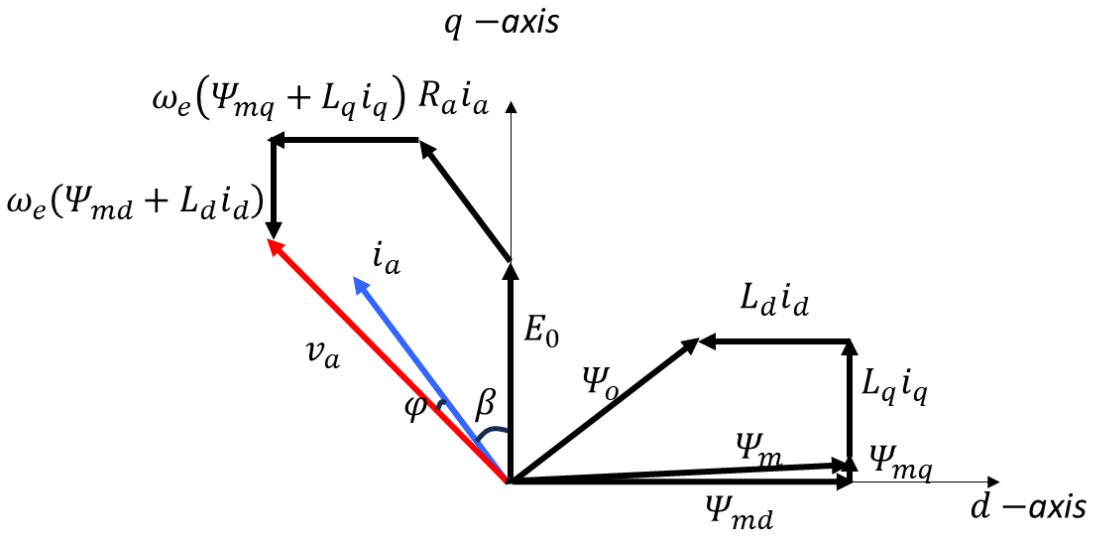


Figure 2.30. IPMSM phasor diagram in d-q axis

Based on this phasor diagram and the d, q-axis equivalent circuit, the voltage equations for the IPMSM can be written as seen in Equation 2.18 to 2.19.

$$v_d = R_a i_d + \omega_e L_d i_d + \omega_e \Psi_{md} \quad \text{Equation 2.19}$$

$$v_q = R_a i_q + \omega_e L_q i_q + \omega_e \Psi_{mq} \quad \text{Equation 2.20}$$

Here, v_d and v_q are d, q-axis voltage, R_a denotes the phase resistance, L_d and L_q are d and q-axis inductance, β is the phase current angle, and φ is the power factor which is angle between voltage and current. Additionally, Ψ_{md} and Ψ_{mq} are the flux density by magnet. The dq transformation is set such that the direction of the magnet flux aligns with the d-axis. Therefore, the q-axis magnet flux Ψ_{mq} typically assumes a value close to zero. However, when under load, the saturation state of the magnetic path, which the flux traverses, is influenced by the armature current, causing changes to this state.

$$i_d = -i_a \sin\beta \quad \text{Equation 2.21}$$

$$i_q = i_a \cos\beta \quad \text{Equation 2.22}$$

$$i_{od} = i_d - i_{cd} \quad \text{Equation 2.23}$$

$$i_{oq} = i_q - i_{cq} \quad \text{Equation 2.24}$$

The formula for the armature current of the IPMSM is represented as shown in Equations 2.20 to 2.23. Here, i_a signifies the peak value of the phase current, while i_d and i_q denote the d-axis and q-axis currents, respectively. Furthermore, i_{od} and i_{oq} represent the values when the iron loss current is excluded. On the other hand, i_{cd} and i_{cq} stand for the equivalent current values, accounting for reductions due to iron loss.

$$T = \frac{3}{2}\frac{n_p}{2}(\Psi_{md} i_d + (L_d - L_q) i_d i_q) \quad \text{Equation 2.25}$$

$$T_m = \frac{3}{2}\frac{n_p}{2}\Psi_{md} i_d \quad \text{Equation 2.26}$$

$$T_r = \frac{3}{2}\frac{n_p}{2}(L_d - L_q) i_d i_q \quad \text{Equation 2.27}$$

Equation 2.24 represents the torque equation of the IPMSM. As outlined in Equations 2.25 and 2.26, this can be further segmented into a magnetic torque component T_m and a reluctance torque component T_r. IPMSM is capable of leveraging the reluctance torque due to the difference in inductance between L_d and L_q. Therefore, controlling the phase angle of the current becomes a crucial factor in the operation of IPMSM.

$$v_d^2 + v_q^2 \leq (V_{om})^2 \qquad \text{Equation 2.28}$$

$$(L_d i_d + \Psi_{md})^2 + \left(L_q i_q\right)^2 \leq \left(\frac{V_{om}}{\omega_e}\right)^2 \qquad \text{Equation 2.29}$$

$$i_d^2 + i_q^2 \leq i_{amax}^2 \qquad \text{Equation 2.30}$$

Equation 2.27 and Equation 2.29 reveal that there is a maximum limit for the voltage V_{om} and current i_{amax} of the motor, which depends on the specifications of the control inverter and the battery. When Equation 2.27 is combined with Equation 2.18 and 2.19, it can be expressed as Equation 2.28. Equation 2.28 represents the form of an ellipse and is referred to as the voltage limit ellipse. On the other hand, Equation 2.29 represents a circle and is known as the current limit circle. Each of these equations signifies the constraints for motor operation, imposed by the limits of the system components such as the inverter and the battery.

Figure 2.21 illustrates the voltage limit ellipse, current limit circle, and the torque line associated with motor drive control. These graphical representations depict the constraints within which the motor operation must adhere. This includes the maximum allowable current, the maximum voltage the system can handle, and the resulting torque the motor can provide, respectively. Understanding these boundaries is crucial to design effective control strategies for efficient motor operation while ensuring the longevity and reliability of the system components. At a given speed, as illustrated in Figure 2.21, it's beneficial to choose the combination of d and q axis currents on the torque line that fulfills the desired torque within the current limit circle while also having the smallest total current value. This method is known as Maximum Torque Per Ampere (MTPA) control. As the speed increases (ω_1, ω_2, and ω_3), the voltage limit ellipse decreases in size as shown in Figure 2.21, and the current combination starts to be influenced by the voltage limit ellipse

at a certain point. At this juncture, the system transitions into operating within the voltage limit ellipse, a state known as Maximum Torque Per Voltage (MTPV) control or field-weakening control. In this mode, even though the current may increase, the total applied voltage stays within the safe operating area, which is crucial at high speeds.

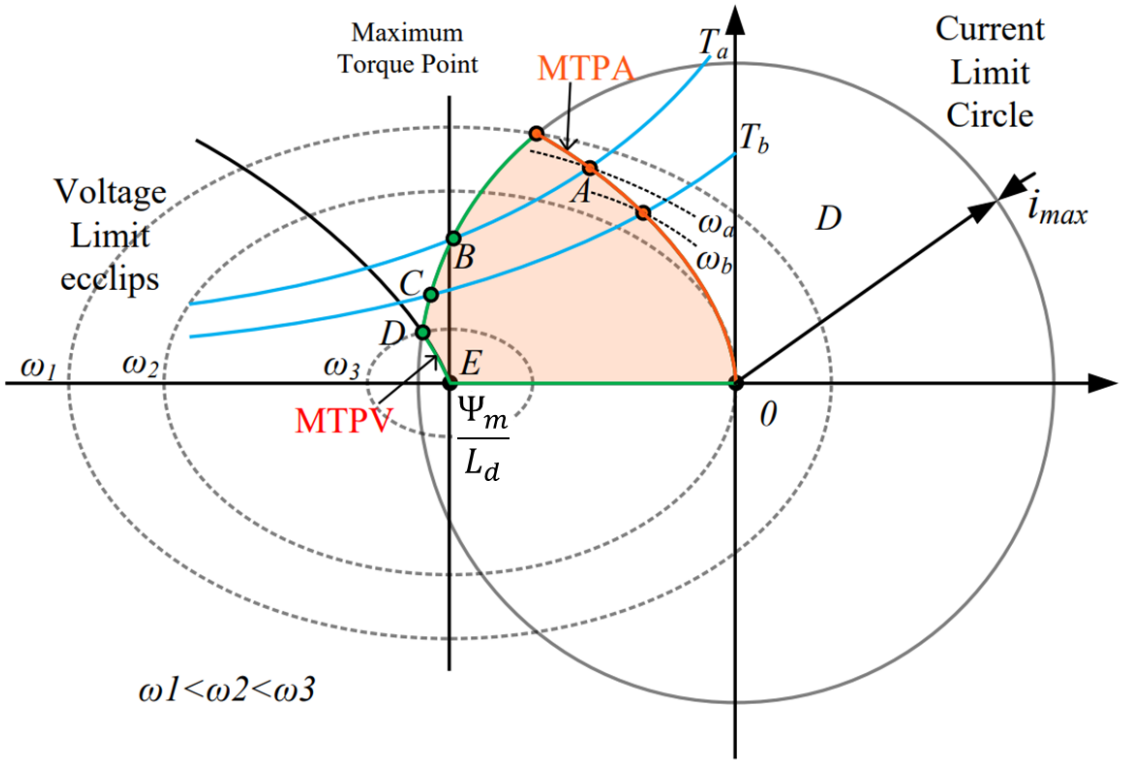


Figure 2.31. Torque, voltage and current depending on speed characteristics of IPMSM in dq-axis.

In this paper, by using MTPA and MTPV control, a method of finding and controlling a current combination that reduces the overall system loss including the loss of the inverter is utilized.

Summary

This chapter has been explored the latest technological research trends aimed at enhancing the efficiency of electric drives. With the rising trend in voltage levels, the multi-level inverter topology reduces the voltage level applied to each device. This enhancement improves control performance and reduces the total harmonic distortion output, resulting

in an overall system loss reduction. Of these, the three-level active neutral point clamped topology offers an advantage due to its ability to utilize a variety of pulse width modulation strategies and balance losses of devices according to the operating conditions.

WBG materials outperform traditional Si devices due to their higher breakdown voltage and superior thermal characteristics. These materials also offer excellent switching characteristics, reducing switching loss. Leveraging these advantages, the use of SiC-MOSFETs as power devices for electric drive inverters is an effective solution.

Furthermore, the IPMSM is a popular choice due to its high speed and high efficiency. This paper discusses a design aimed at reducing energy loss using a 3L-ANPC topology, a SiC-MOSFET as a WBG material, and an IPMSM.

3 Energy Efficient Design Target

This chapter deals with the design methodology for energy-efficient electric drives, leveraging the cutting-edge research on inverters and machines discussed in the preceding chapter. The pivotal objective when defining targets for inverter-machine co-design focus on total energy consumption. The goal is to minimize overall energy consumption for an identical EV traction system under given driving conditions. Merely comparing the maximum or average efficiency of the system is not a beneficial metric. A system with high maximum efficiency may hold less importance if the point of peak efficiency falls within a rarely operated area in practical terms. Thus, the most frequently operated area should be identified, the total system loss including inverter and machine considering co-effect at the corresponding point based on this profile is calculated, and the optimal design approach capable of minimizing this sum of energy loss is presented in this chapter.

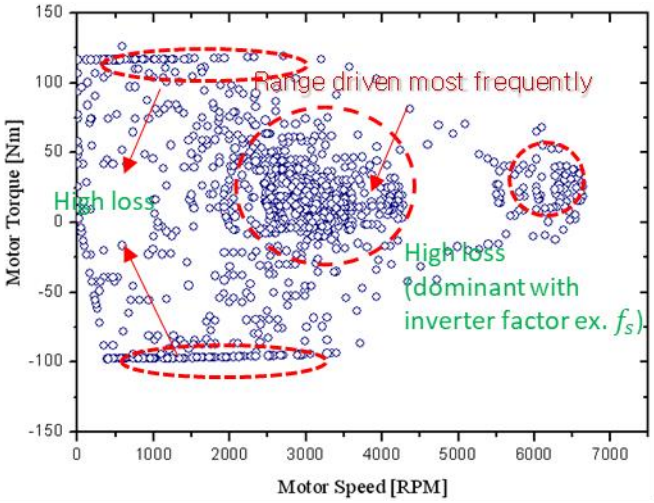


Figure 3.32. Example of most frequent operating region of electric drive

3.1 Total Energy Consumption During the Drive Cycle

3.1.1 Various Drive Cycle for Vehicle Evaluation

Drive cycles, which serve as standards for assessing fuel economy or greenhouse gas emission levels, are a good source for identifying frequently used conditions. Different countries adhere to different standards, with the New European Driving Cycle (NEDC) and

the Worldwide Harmonized Light Vehicles Test Procedure (WLTP) being the most widely adopted in Europe, while the United States follows the standards set by the Environmental Protection Agency (EPA). The NEDC protocol was introduced in 1992 and has seen widespread use [77,78]. However, due to the need for an improved measurement method, the United Nations Economic Commission for Europe (UNECE) Inland Transport Committee decided to replace it with WLTP in 2017 [79]. Compared to the NEDC, the WLTP more accurately reflects real road conditions and driver behavior; it has higher average and maximum speeds, simulates longer distances, and includes steeper acceleration and deceleration conditions. Among the various classes of WLTP, electric vehicles follow class 3. Figure 3.2 shows the vehicle profiles for NEDC and WLTP class 3, with approximate conditions listed in Table 3.1.

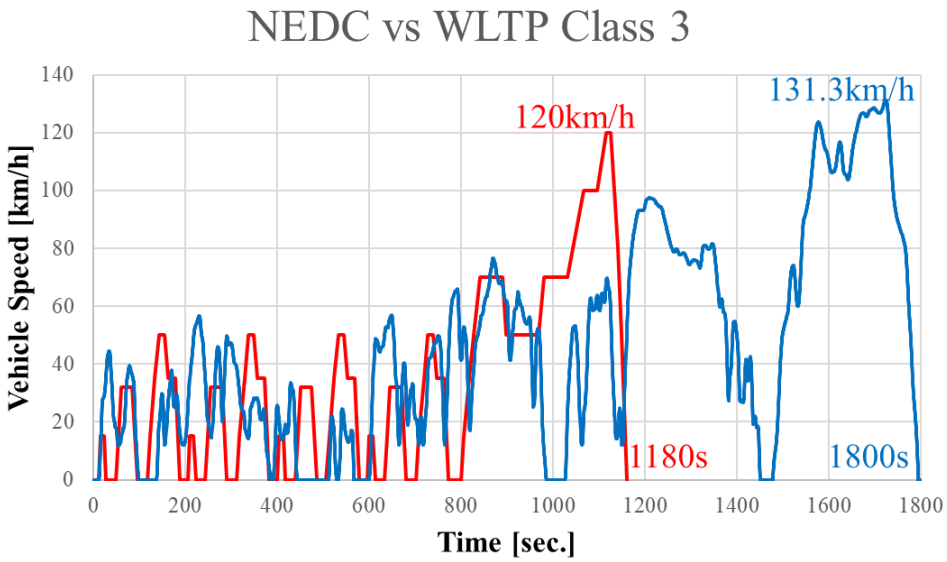


Figure 3.33 Example of most frequent operating region of electric drive

Table 3.7. Comparison of drive cycle (NEDC vs WLTP)

Item	**NEDC**	**WLTP**
Cycle Time [min.]	20	3.2
Distance [km]	11	23.25
Maximum Dpeed [km/h]	120	131.1
Average Speed [km/h]	34	46.5
Driving Phase	2 (urban: 66% / highway: 34%)	4 (urban: 52% / highway: 48%)
Stop Time [%]	24	12.5

In the United States, the EPA standards are followed, with the most representative ones being the FTP-75 conditions, reflecting city driving, and the Highway Fuel Economy Test (HWFET), simulating highway driving [80]. A blend of these two cycles is often used. There are also other cycles like the US06 [81], which features severe acceleration and deceleration, and the SC03, which involves the use of an air conditioner [82].

3.1.2 Electric Drive Profile Calculation

In transforming the vehicle profile of the drive cycle into the electric drive profile of the inverter and machine, the longitudinal dynamics of the vehicle are a crucial factor that needs to be accounted for [83]. This representation of longitudinal dynamics is demonstrated in Figure 3.3. The driving force, F_{drive} required to set a vehicle in motion needs to balance several counteracting forces. These include the forces attributable to acceleration, F_m, rolling resistance, F_r, aerodynamic drag, F_a, and the climbing gradient force F_c. Each of these forces can be determined by utilizing a series of equations, specifically Eq 3.1-3.5, where θ_e is the climbing gradient, and g represents gravitational acceleration. This conversion process is pivotal in translating real-world driving conditions into electrical parameters that can guide the design and optimization of power electronics and electric motor systems. The consideration of longitudinal dynamics thus provides a more accurate and realistic representation of the operation conditions these systems will encounter, enabling a more effective design process.

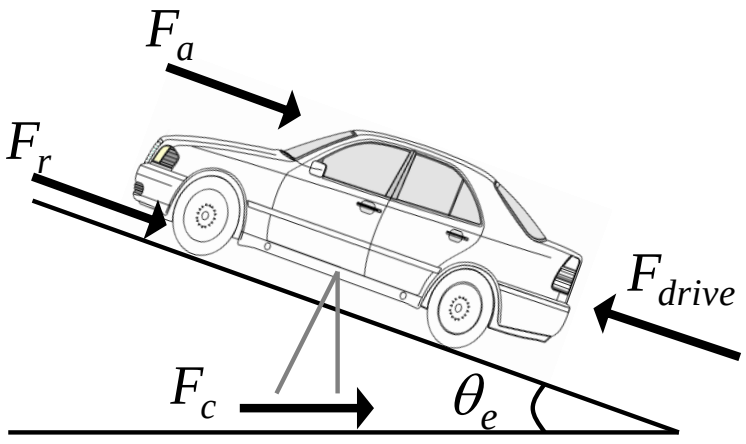


Figure 3.34 Longitudinal dynamics of vehicle

$$F_{drive} = F_m + F_r + F_a + F_c \quad \text{Equation 3.1}$$

$$F_m = \left(M_v + \frac{I_m \cdot G^2 \cdot \eta_g}{TDR^2}\right) \cdot a_v \quad \text{Equation 3.2}$$

$$F_r = C_{rr} \cdot M_v \cdot g \cdot \cos\theta_e \quad \text{Equation 3.3}$$

$$F_a = \frac{1}{2}\rho \cdot A_F \cdot C_d \cdot v_v^2 \quad \text{Equation 3.4}$$

$$F_c = M_v \cdot g \cdot \sin\theta_e \quad \text{Equation 3.5}$$

The driving force acting on the wheels and given parameters of the vehicle such as the tire dynamic radius[2] or the vehicle weight, the output torque, T_m and rotational speed of the machine, ω_m can be calculated. These can be found using Eq. 3.6 and Eq. 3.7, respectively. Table 3.2 shows an example of a typical vehicle specification.

Table 3.8. Vehicle specifications.

Item	**Vehicle specification**
Vehicle weight, M_v [kg]	2,050
Motor inertia, I_m [kg-m^2]	0.0025
Gear ratio, G	9.18
Gear efficiency, η_g[%]	97
Tire dynamic radius, *TDR* [m]	0.35
Rolling resistance coefficient, C_{rr}	0.008
Air-drag resistance coefficient, C_d	0.21
Air density, ρ [kg/m^3]	1.25
Frontal area, A_F [m^2]	2.1
Vehicle speed, v_v [m/s]	Profile
Vehicle acceleration, a_v [m/s^2]	Profile
Regenerative brake ratio [%]	70 (estimation)

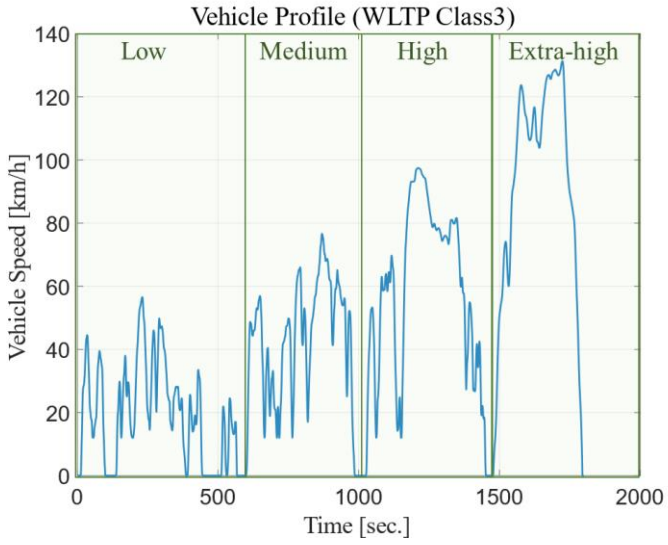
$$\omega_m = v_v \cdot \frac{G}{TDR} \quad \text{Equation 3.6}$$

$$T_m = F_{drive} \cdot \frac{TDR}{G}\frac{1}{\eta_g} \quad \text{Equation 3.7}$$

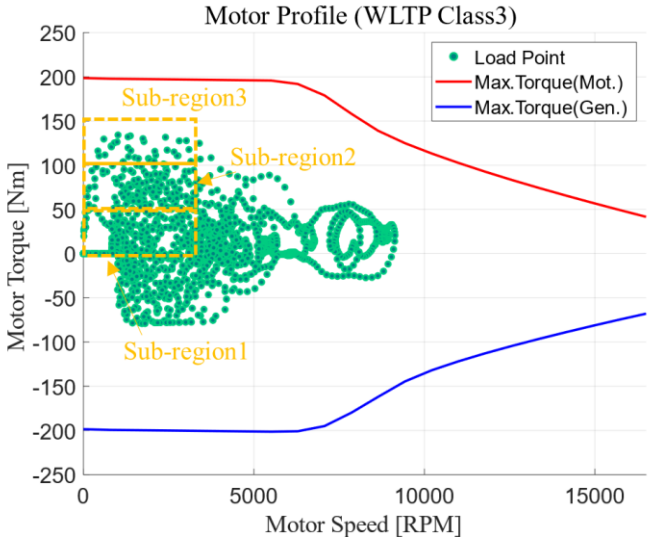
[2] In vehicular dynamics, due to variations in motion conditions, the dynamic radius of the tire is employed instead of the static radius

Approaches exist for establishing the speed boundary at which regenerative braking is possible, based on the performance curve of the motor, and for adjusting friction-based brakes and regenerative brakes to optimize energy output [84,85]. However, For the purpose of simplifying the calculations and explaining the methodology in this paper, it is assumed that regenerative braking maintains a constant value throughout the entire cycle.

The electric drive profile, calculated from the WLTP class 3 drive cycle through the process mentioned above, is depicted in Figure 3.4.



(a)



(b)

Figure 3.35. WLTP class 3 drive cycle (a) vehicle profile (time-speed) (b) traction electric drive profile (rotational speed-torque)

3.1.3 Energy Gravity Center Method

As illustrated in Figure 3.4, an interesting observation can be made: with the increase in complexity and duration time of the vehicle drive cycle, there is a corresponding increase in the operational points on the rotational speed-torque profile as depicted by green dot. Accounting for all these points, computing the losses at each load point for the electric drive, and setting optimization targets for them can be a time-consuming and resource-intensive task. This is especially true during the initial phases of the design process, where such an approach can prove to be notably inefficient. Therefore, an alternative approach can be adopted as demonstrated in Figure 3.4 (b). Here, it can be seen that each load point divided into various sub-regions based on specific speed and torque. Once this is done, a representative point for each of these sub-regions can be selected. With the utilization of the energy center of gravity method [86], it's possible to derive the speed at the energy gravity center point, ω_{mci} and torque at the same point, T_{mci} that satisfy the conditions set forth by Eq 3.5 to 3.7. N_i denotes the quantity of points in the i^{th} sub-region, and E_{mi} signifies the energy of the i^{th} region. One crucial factor that must not be overlooked during this process is the duration time for each load point, which also needs to be considered.

$$E_{mi} = \sum_{j=1,2,\dots}^{N_i} E_{mij} \qquad \text{Equation 3.8}$$

$$n_{mci} = \frac{1}{E_{mi}} \sum_{j=1,2,\dots}^{N_i} E_{mij} n_{mij} \qquad \text{Equation 3.9}$$

$$T_{mci} = \frac{1}{E_{mi}} \sum_{j=1,2,\dots}^{N_i} E_{mij} T_{mij} \qquad \text{Equation 3.10}$$

As the number of sub-regions increases, though a wider variety of load points can be accurately represented, the computational effort required also rises proportionately. To illustrate this point, Figure 3.5 presents the calculated total loss value according to the number of defined sub-regions. Additionally, this figure shows the error defined by the difference between the calculated total loss by all drive cycle point (depicted by green dot in Figure 3.4 (b)) and the one by different number of representative points. This analysis demonstrates that a relatively small error, less than 3%, is observed when more than 10 points are chosen. Therefore, in this example, it is considered appropriate to select a

minimum of 10 points for accurate estimation of the drive cycle losses. Selecting a number exceeding 10 points could require additional computational effort, and as such, an optimum 10 points are targeted for the design. This figure may vary depending on the specific drive cycle and the electric drive model under consideration.

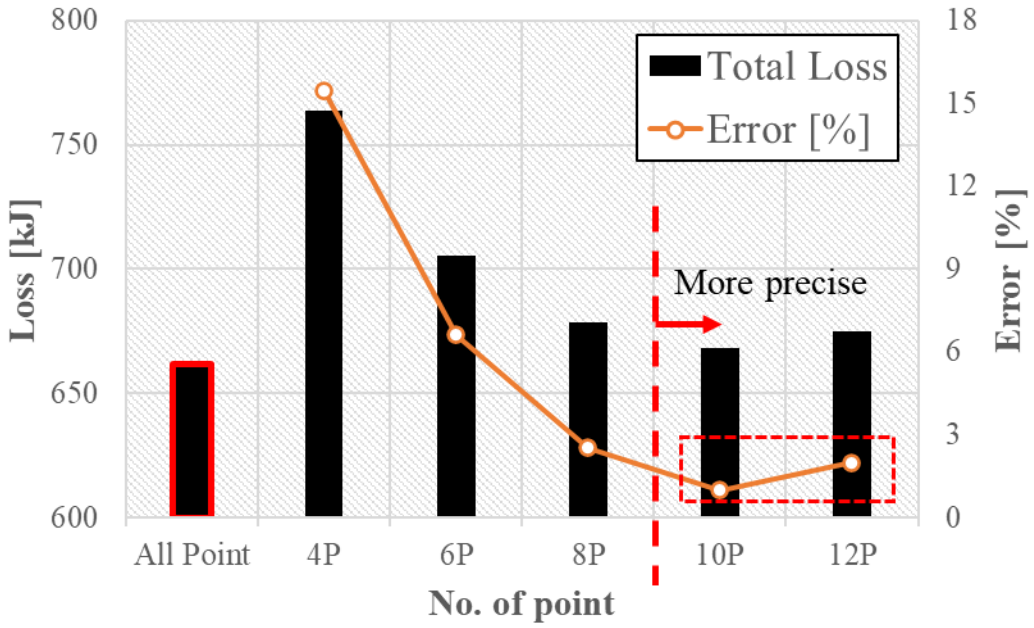


Figure 3.36 Calculated loss and error between energy gravity center with different no. of point and all drive cycle points.

The result of this comprehensive process, involving the calculation of ten representative points from these sub-regions, is shown in Figure 3.6. By performing the optimization design using these ten representative points, computational efficiency can be enhanced, that means the total energy loss consumption during the drive cycle can be computed with minimal effort of time and resource. This approach allows for a swift, efficient computation while maintaining a high level of accuracy in the energy loss predictions. The technique allows for a more manageable amount of data to be processed, which simplifies the overall design and optimization process. This way, engineers can focus more on refining the performance of the system and enhancing the electric drive's energy efficiency.

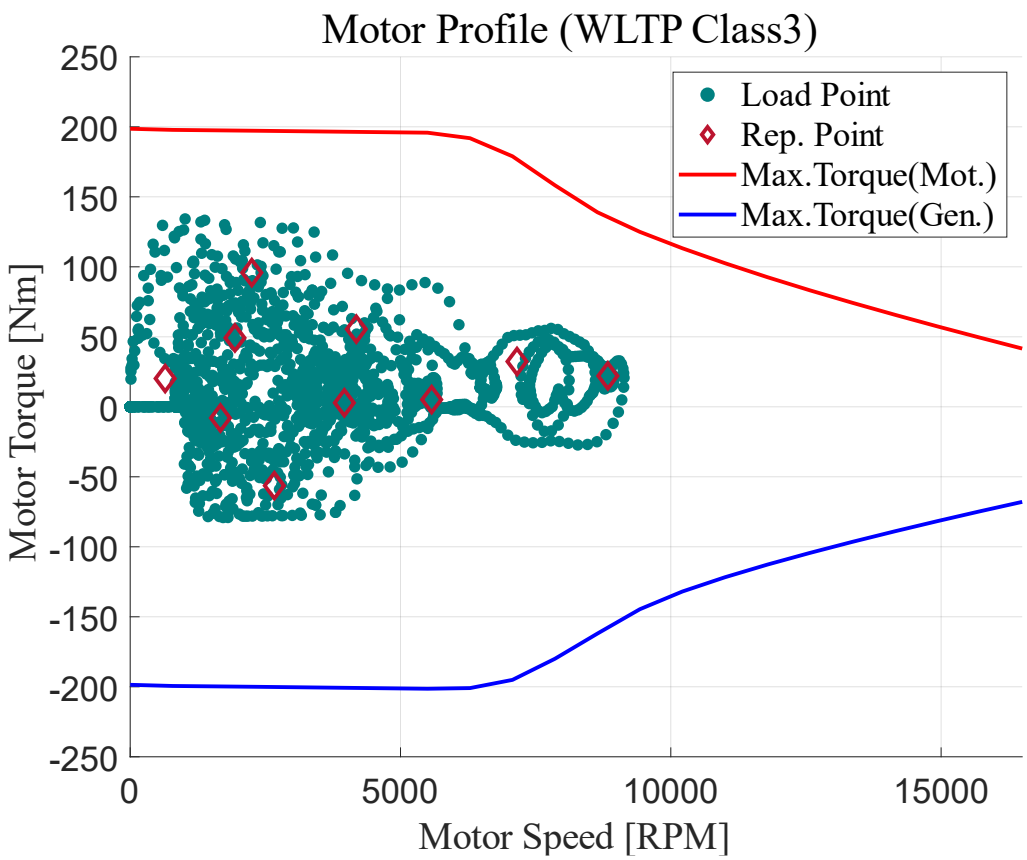


Figure 3.37 Ten representative operational points calculated by energy center gravity.

3.2 Overall Power Loss Calculation

By assessing the energy loss at these typical load points, derived from calculating the losses of the inverter and motor as depicted in Figure 1.5, the total energy loss consumption over the entire drive cycle, E_{cycle} can be calculated. The ultimate objective function for the design methodology explored in this paper can be articulated as per Eq. 3.12 and Eq. 3.13, where P_{ED} is the total losses of the electric drive, P_{cond} and P_{sw} denote the conduction and switching losses of the inverter, and P_{CU}, P_{iron}, and P_{mag} presents the copper losses, iron losses, and magnet eddy current losses of the machine. This chapter will delve into the theoretical approach applied to each loss component of both the inverter and the motor.

$$E_{cycle} = \int_{cycle} P_{ED}\, dt \qquad \text{Equation 3.11}$$

$$P_{ED} = P_{cond} + P_{sw} + P_{CU} + P_{iron} + P_{mag} \quad \text{Equation 3.12}$$

3.2.1 Conduction Loss

Conduction losses are the losses that result from the current flowing through the switch device during its on-state, as well as from the freewheeling diode current that flows through the body diode or antiparallel diode during the dead-time. It can be computed by multiplying the on-state voltage and on-state current [87-89]. This is defined as Equation 3.14, 3.15, and 3.16. Here, P_{cond_MOS}, P_{cond_IGBT}, and P_{cond_Diode} refers to the conduction losses of MOSFET, IGBT, and diode. $I(\theta)$ is the current flowing through the deivces; drain current in the case of MOSFET, collector current for the IGBT, and diode current.

$$P_{cond\_MOS} = I(\theta)^2 R_{DS} \quad \text{Equation 3.13}$$

$$P_{cond\_IGBT} = I(\theta)V_{CE0} + I(\theta)^2 R_{CE} \quad \text{Equation 3.14}$$

$$P_{cond\_\text{Diode}} = I(\theta)V_{F0} + I(\theta)^2 R_F \quad \text{Equation 3.15}$$

$$R_{CE} = \frac{\Delta V_{CE}}{\Delta I_C} \quad \text{Equation 3.16}$$

$$R_F = \frac{\Delta V_F}{\Delta I_F} \quad \text{Equation 3.17}$$

Figure 3.7 provided the typical voltage-current characteristics of MOSFETs, IGBTs, and anti-parallel diodes. Starting with MOSFETs in (a), it can be observed that when a gate-source voltage exceeds a certain threshold, the voltage-current characteristic approximates a linear relationship. This allows us to calculate the conduction loss using the on-state drain-source resistance R_{DS} as shown in Equation 3.14. In the cases of IGBT in (b) and diode in (c), the characteristic curves can also be approximated as linear after a specific voltage value. In the IGBT scenario, V_{CE0} refers to the on-state voltage threshold, and R_{CE} represents the on-state resistance, which is defined by Equation 3.17, and derived from the slope of the curve depicted in Figure 3.7 (b). Likewise, for a diode, the forward voltage threshold V_{F0} and the curve's slope in (c) are used to calculate the forward resistance value R_F as Equation 3.18. The cumulative total of these losses accounts for the conduction loss of a single power device set over the course of an entire cycle.

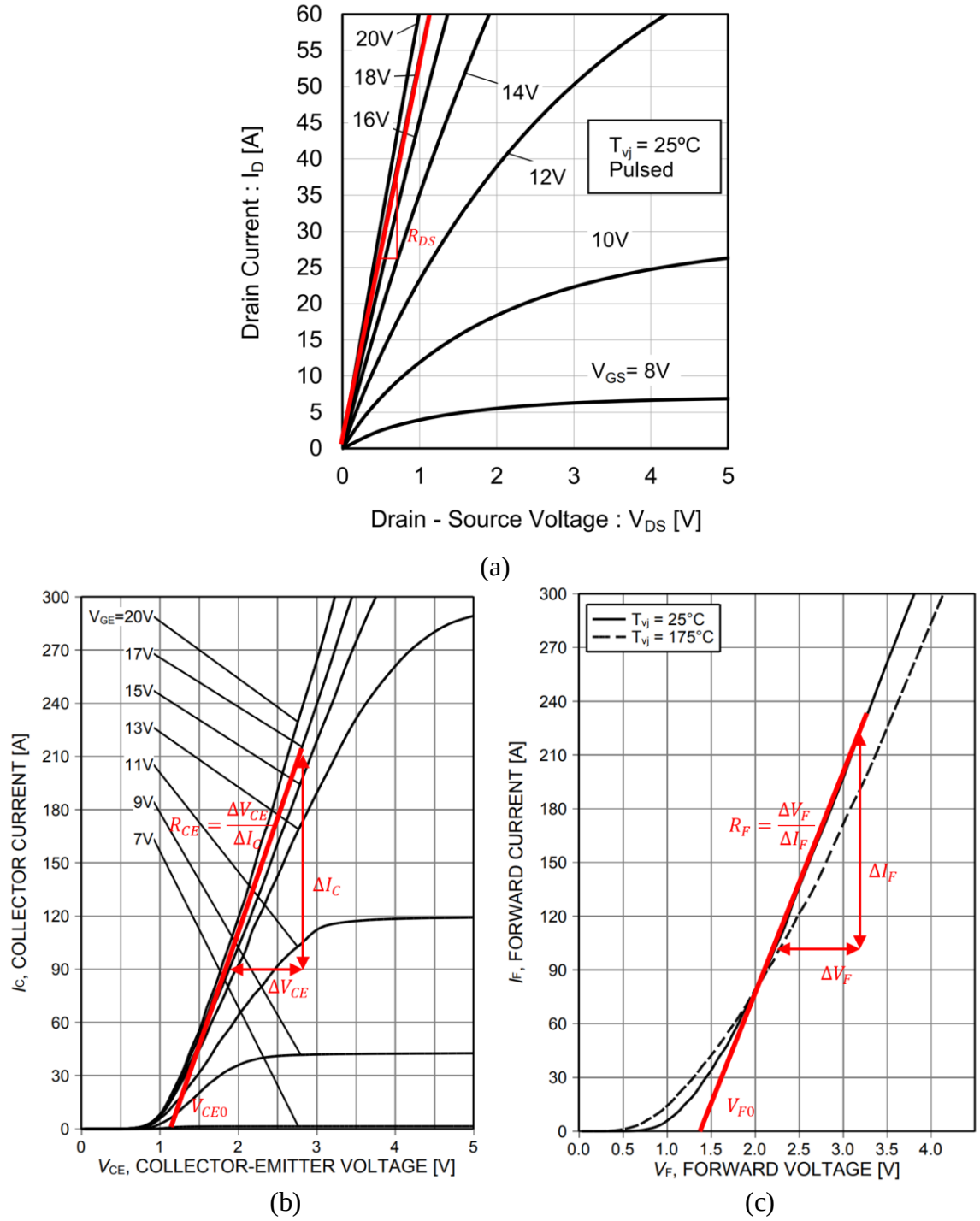


Figure 3.38 Typical voltage-current characteristics of (a) MOSFETs (b) IGBTs (c) diodes, modified from the datasheet [90,91].

3.2.2 Switching Loss

Switching losses in a MOSFET are one of the primary factors influencing its overall efficiency. These losses occur during the transition periods when the device is turning on or off. Figure 3.8 shows the drain-source voltage and drain current waveform during switching on/off-states.

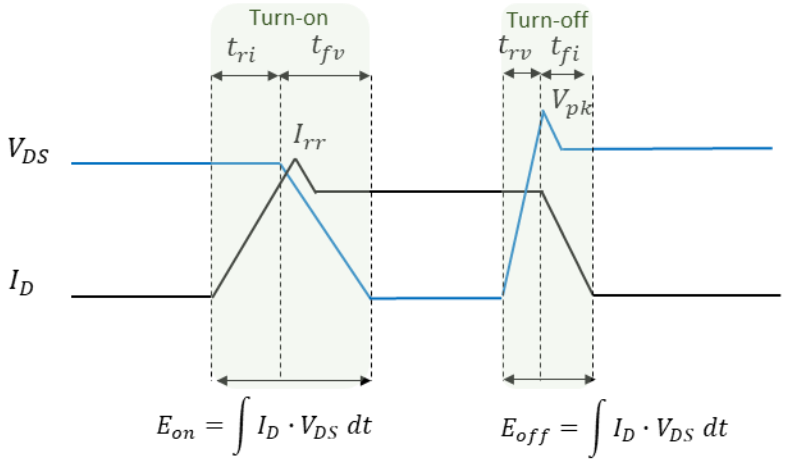


Figure 3.39 Typical waveform of the drain-source voltage and drain current during switch turn-on and turn-off.

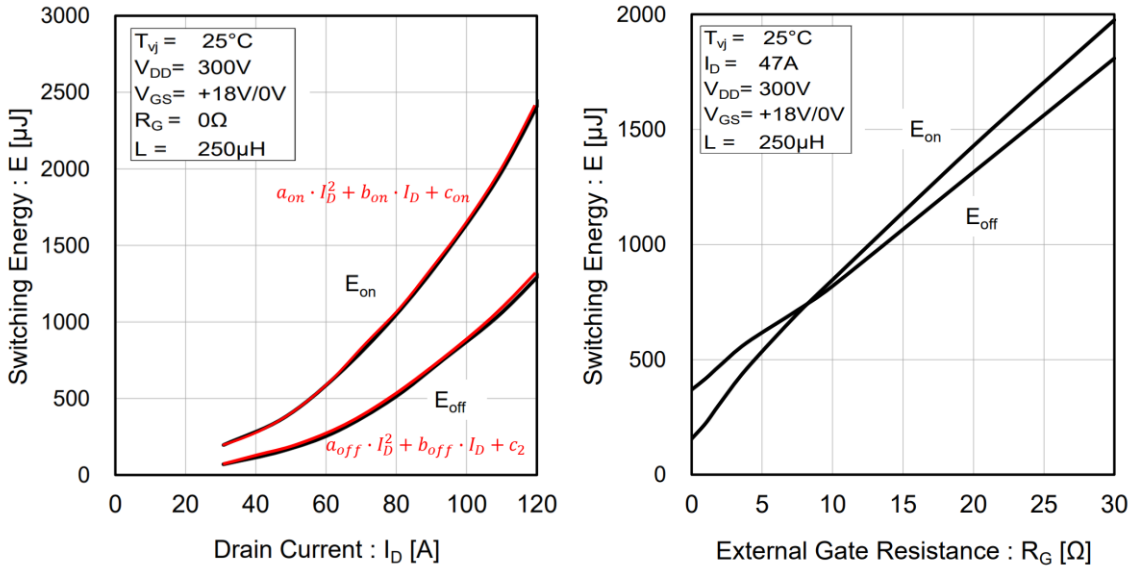
The total switching loss in a MOSFET can be divided into two main components: turn-on losses and turn-off losses. Turn-on losses occur when the transistor transitions from an off-state to an on-state. During this period, the voltage across the drain and source V_{DS} of the MOSFET decreases from its maximum to nearly zero, while the drain current I_D rises from zero to its maximum. The product of V_{DS} and I_D during this transition period is the turn-on loss. The area under the power versus time curve during the turn-on phase represents this loss. The turn-on switching energy, Eon is like as Eq. 3.20, where I_{rr} is the diode reverse recovery current, t_{ri} is the current rise time and t_{fv} is the voltage fall time.

$$E_{on} = \frac{1}{2} V_{DS} \cdot (I_D + I_{rr}) \cdot t_{ri} + \frac{1}{2} V_{DS} \cdot \left(I_D + \frac{2}{3} I_{rr}\right) \cdot t_{fv} \qquad \text{Equation 3.18}$$

Conversely, turn-off losses occur when the transistor transitions from an on state to an off state. In this case, I_D decreases from its maximum value to zero while V_{DS} rises from close to zero to its maximum. Again, the product of V_{DS} and I_D during this transition period gives the turn-off loss.

$$E_{off} = \frac{1}{2} V_{DS} \cdot I_D \cdot t_{rv} + \frac{1}{2}\left(V_{DS} + V_{pk}\right) \cdot I_D \cdot t_{fi} \qquad \text{Equation 3.19}$$

Total switching loss is simply the sum of the turn-on and turn-off losses. It's important to note that the rate of change of the current and voltage (*di/dt* and *dv/dt*) during these transitions greatly influences these losses. Faster switching speeds can reduce switching losses but can also lead to other issues such as increased electromagnetic interference (EMI). Most datasheets for power devices provide typical values for turn-on and turn-off states, which can be used for an approximate calculation of switching losses [90,91]. From the datasheet, the switching energy during turn-on and turn-off states can be modelled as a function of drain current I_D as depicted by Figure 3.9 (a). The coefficient *a*, *b*, and *c* for each state (on and off) can be determined by second-order curve fitting method. As can be seen in Figure 3.9 (b), it's important to note that the switching energy is also influenced by external gate voltage and drain-source voltage. Therefore, the coefficient for these factors should be modified accordingly. Generally, E_{on} and E_{off} are proportional to drain-source voltage value, so it can be computed by Equation 3.23 and 3.24, where V_{REF} denotes the reference voltage when the switching energy is measured in datasheet.



(a) (b)

Figure 3.40 Typical switching energy (a) depending on i_D (b) depending on external gate resistance, modified from the datasheet [90,91].

$$P_{sw} = \left(E_{on} + E_{off}\right) \cdot f_s \qquad \text{Equation 3.20}$$

$$E_{on} = \left[a_{on} \cdot I_D^2 + b_{on} \cdot I_D + c_{on}\right] \frac{V_{DS}}{V_{REF}} \qquad \text{Equation 3.21}$$

$$E_{off} = \left[a_{off} \cdot I_D^2 + b_{off} \cdot I_D + c_2\right] \frac{V_{DS}}{V_{REF}} \qquad \text{Equation 3.22}$$

3.2.3 Analytical Loss Calculation of 3L-ANPC

Comparing PWM strategies by calculating switching losses and conduction losses in an analytical way based on various PWM strategies for 3L-ANPC inverters covered in Chapter 2.1.2.

In this analysis, the PWM strategies explored in Tables 2.3, 2.4, and 2.5 are considered. Figure 3.10 illustrates the switching sequence for each device as per each PWM strategy.

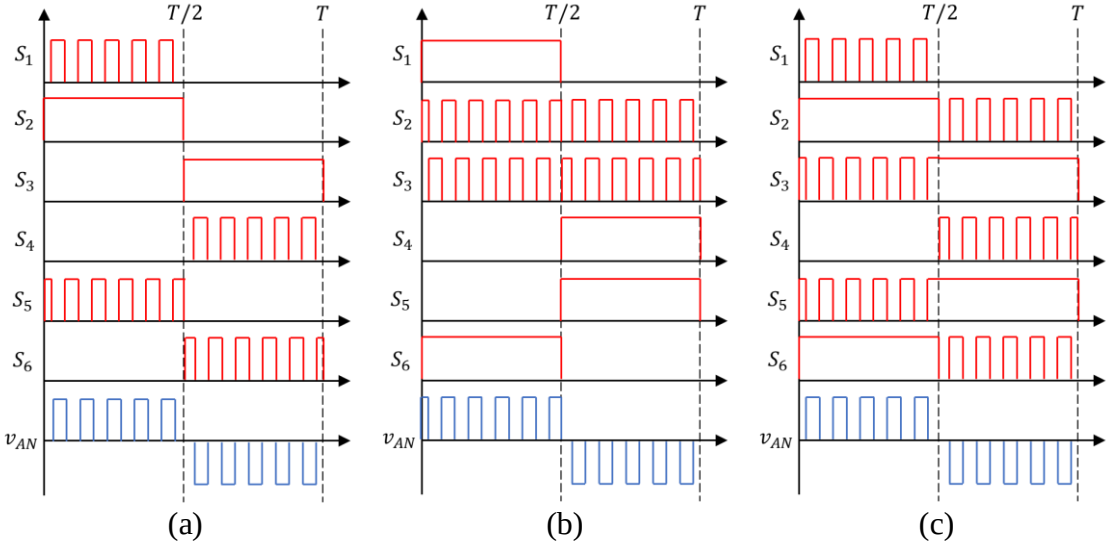


Figure 3.41 Modulation strategies and corresponding switching sequence (a) PWM1 (b) PWM2 (c) PWM3.

For PWM1, the current flows along a short current path in the zero state, and the strategy for implementation is depicted in Figure 3.10 (a). Here, S2 and S3 switch at the line frequency, while the remaining four devices switch at a high switching frequency for half the period. Therefore, this strategy can be optimal for a 4SiC-2Si hybrid topology where the four switches, other than S2 and S3, are replaced with SiC and S2 and S3

utilize Si-IGBTs. In this manner, losses can be reduced by capitalizing on the superior switching characteristics of SiC. Since S2 and S3 do not exhibit high switching losses, Si-IGBTs with favorable conduction characteristics can be chosen.

For PWM2, as depicted in Figure 3.10 (b), high-frequency switching is concentrated on the two devices nearest to the load. Only S2 and S3 are switching at high frequency, and the other four devices are almost not switching. This can be effective as it may reduce the overall switching loss in the region where switching loss is dominant. However, there might be a loss imbalance as losses are concentrated in S2 and S3. Nevertheless, this could also be addressed by replacing S2 and S3 with SiC devices, which have a smaller switching loss, thus creating a 2SiC-4Si hybrid topology.

The final strategy to consider is PWM3. As illustrated in Figure 3.10 (c), all six switches perform high-frequency switching. However, in the zero state, the current path is distributed across both top and bottom—that is, between a short loop and a long loop—hence, conduction loss can be minimized. This may be beneficial in regions or applications where conduction losses are more significant than switching losses. Compared to the previous two PWM strategies, the losses are most evenly distributed across each power device in PWM3. Also, there's only one zero state, and the states of 0+ and 0- are identical.

In order to calculate losses analytically for these three PWM strategies, several simplifying assumptions are used. 1) Current ripple effects are disregarded when calculating the current using the averaged method. 2) The effect of dead time is also disregarded. 3) A single-phase state is assumed, and the SPWM method is used to simplify the calculations

Figure 3.11 shows the modulation signal and output current in a specific state in the PWM3 strategy, and the current flowing through S2 and the gate control signal. In (a), phase angle φ is the angle between modulation signal and phase current, and m is the modulation index. The power factor is equal to the modulation signal. For each switch device, the modulation signal varies according to the PWM strategy, and as a result, the current flowing through each device and the gate signal differs as well. As illustrated in (b), positive current flows through the drain or collector of S2, whereas negative current signifies a flow through the body-diode or anti-parallel diode. Therefore, depending on the

PWM strategy and phase angle, the current sections that flow through the switching device and the diode can be computed.

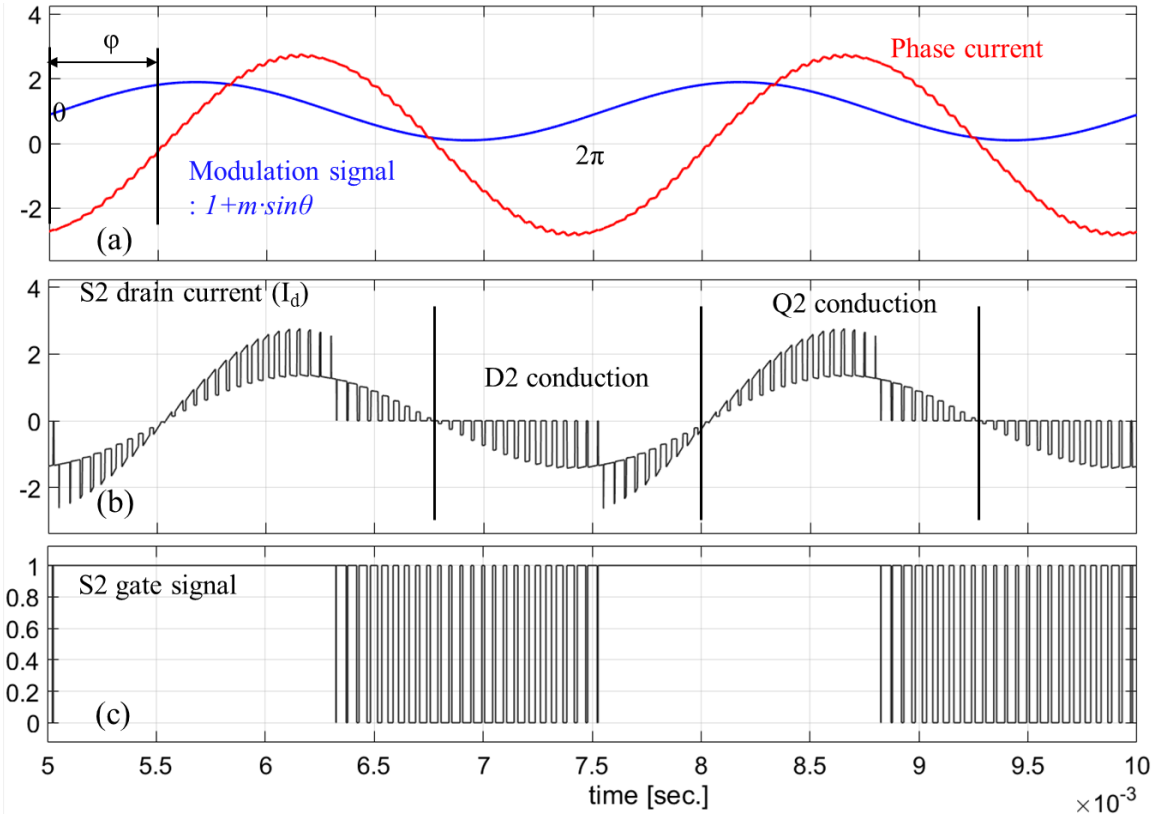


Figure 3.42 Conduction and switching loss interval for calculation (a) modulation signal, phase current, and phase angle (b) S2 drain current (c) S2 gate signal.

From Equations 3.14, 3.15, and 3.16, the conduction loss through the switching device can be calculated using the average value of the current, as described in Equation 3.25 and 3.26. Here, P_{cond_Q} refers to the conduction loss of the IGBT or MOSFET, and P_{cond_D} represents the conduction loss of the diode. V_0 is the knee voltage, for the MOSFET, this value is generally zero, but for IGBT device, this should be considered by V_{CE0} in Equation 3.15.

$$P_{cond\_Q} = \frac{1}{2\pi}\int \left[R_{DS}\left(I_{pk}\sin(\theta-\varphi)\right)^2 + V_0 I_{pk}\sin(\theta-\varphi)\right] s(\theta)d\theta \qquad \text{Equation 3.23}$$

$$P_{cond\_D} = \frac{1}{2\pi}\int \left[R_{DS}\left(-I_{pk}\sin(\theta-\varphi)\right)^2 - V_0 I_{pk}\sin(\theta-\varphi)\right] s(\theta)d\theta \qquad \text{Equation 3.24}$$

In Fig. 3.11 (b), the conduction loss of S2 in the PWM3 strategy is calculated using integration range [φ, π+φ] for Equation 3.25, and [0, φ] for equation 3.26. Similarly, by

calculating the conduction intervals, tthe conduction loss for each of the six devices under each PWM strategy can be calculated.

Switching loss can be modelled as second-order polynomial, from datasheet graph as seen in Figure 3.9 (a). In this case, each coefficient can be obtained from one total switching loss without separating turn-on loss and turn-off loss as in 3.23 and 3.24. That is, it is calculated by merging 3.23 and 3.24. The switching loss can be obtained from Equation 3.27. The *a*, *b*, and *c* coefficients are approximate coefficients of the total loss energy. The voltage applied to power device in 3L-ANPC inverter topology is half of DC-link voltage, so $V_{DC}/2$ value is used in Equation 3.27.

$$P_{sw} = \left[\frac{1}{2\pi}\int \left[a\left(I_{pk}\, sin(\theta-\varphi)\right)^2 + bI_{pk}\, sin(\theta-\varphi) + c\right] d\theta\right]\frac{V_{DC}/2}{V_{ref}} f_s \qquad \text{Equation 3.25}$$

Figure 3.12 shows the results of calculating the loss when PF=*1*, PF=-*1*, and PF=*0* using the CM30015065D SiC MOSFET [92]. In the case of PWM3, the loss distribution is most evenly spread out, and it also results in the smallest total loss, making it the most efficient. PWM1 and PWM2 have similar combined losses, but the distribution of loss across each device differs depending on the PWM strategy. Thus, the PWM strategy can be analyzed under various load conditions.

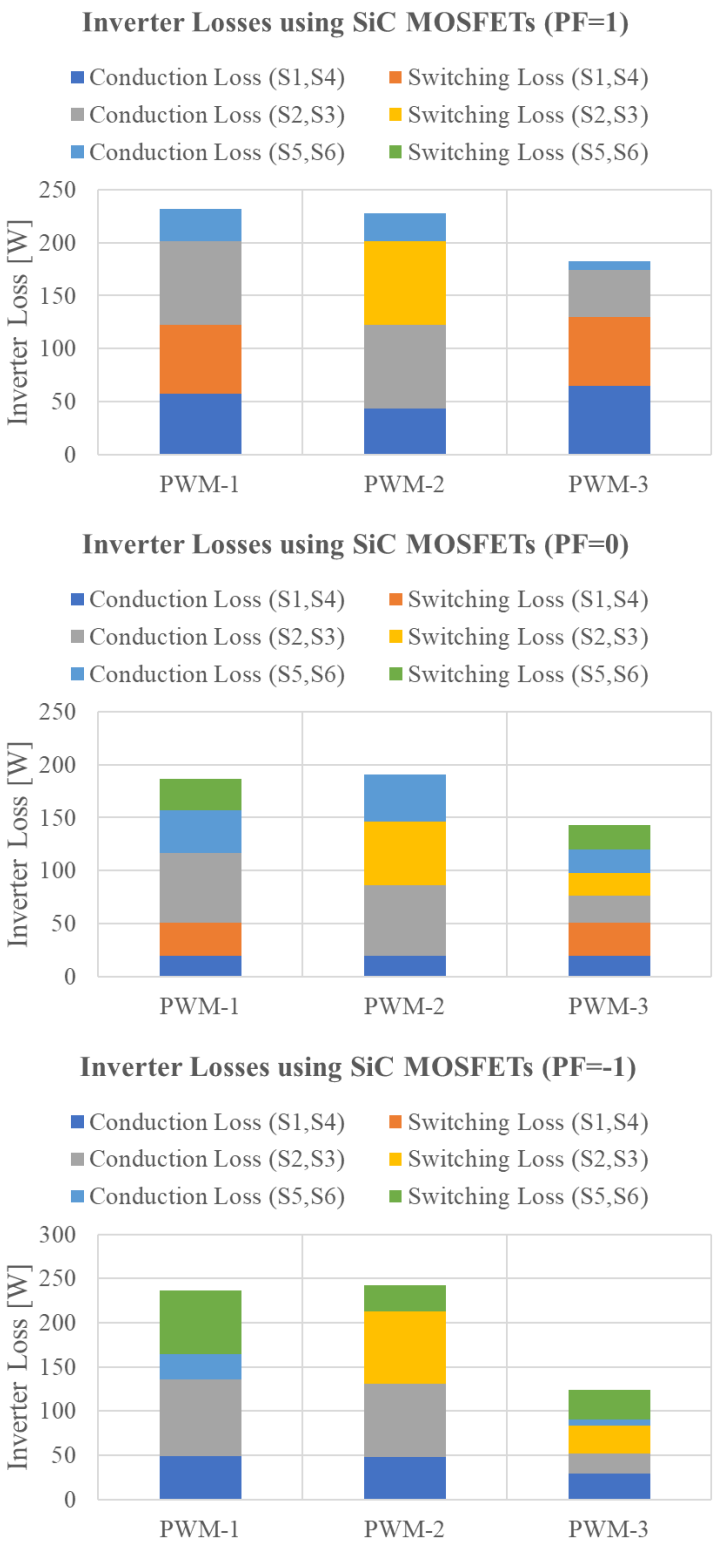


Figure 3.43 Conduction and switching loss calculation results with different PWM strategies (a) PF = 1 (b) PF = 0 (c) PF=-1.

3.2.4 Joule Loss

Copper loss, a significant type of loss in a motor, refers to the conduction loss that arises from the current passing through the motor winding. Copper loss is proportional to the product of the square of the current flowing in the coil and the winding resistance. The resistance in a DC state, where the current value remains constant over time, is depicted in Equation 3.28. Here, ρ_{CU} is resistivity of copper, l_{stk} denotes stack length, l_{enT} presents the end-turn length, A_{coil} and n_T are the cross area of the coil and number of series turn per phase. α and T are the temperature coefficient of resistivity and operating temperature.

$$R_{DC} = \rho_{CU} \frac{2(l_{stk}+l_{end})}{A_{coil}} n_T \cdot [1 + \alpha \cdot (T - 20℃)] \quad \text{Equation 3.26}$$

However, in practice, the magnitude of the current flowing in the coil winding changes depending on the frequency, and the larger the current ripple, the higher the frequency of current alternation. In this situation, the resistance of the conductor increases due to the proximity effect and skin effect as can be seen in Figure 3.13 [93].

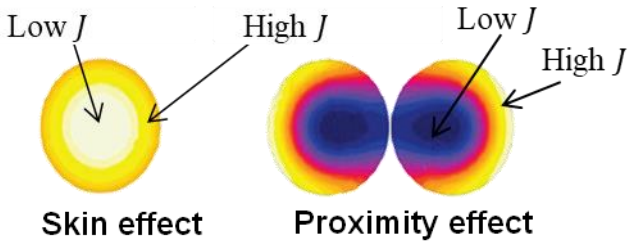


Figure 3.44 Concept of the skin effect and proximity effect.

The AC copper loss, which fluctuates based on frequency, can be determined as illustrated in Equation 3.29 by computing the AC loss factor, K_{AC} for the DC resistance acquired in Equation 3.28.

$$R_{AC} = R_{DC} \cdot K_{AC}(\eta) \quad \text{Equation 3.27}$$

To determine the AC loss factor K_{AC} of rectangular winding, first find the characteristic dimension η, using the layer fill factor ϵ_l and skin depth δ, as demonstrated in Equations 3.30 to 3.32 [94]. In this context, h_c is conductor height, w_c is conductor width, σ is electrical conductivity, f is frequency, and μ_0 is the free space permeability.

$$\eta = \sqrt{\epsilon_l} \cdot \frac{h_c}{\delta}$$ Equation 3.28

$$\epsilon_l = \frac{N(w_c h_C)}{w_l h_c}$$ Equation 3.29

$$\delta = \sqrt{\frac{1}{\pi f \mu_0 \sigma}}$$ Equation 3.30

Utilizing a layer conductor model, where resistance varies with each layer due to alternations in the magnetic field, the AC loss factor can be computed as illustrated in Equation 3.33, where C_I and C_{II} are defined in Equation 3.34 and 3.35.

$$K_{AC} = C_I(\eta) + \frac{C_{II}(\eta)}{N} \sum_{i=1}^{N} (2n-1)^2$$ Equation 3.31

$$C_I(\eta) = \frac{\eta \sinh(\eta) + \sin(\eta)}{2\cosh(\eta) - \cos(\eta)}$$ Equation 3.32

$$C_{II}(\eta) = \frac{\eta \sinh(\eta) - \sin(\eta)}{2\cosh(\eta) + \cos(\eta)}$$ Equation 3.33

Figure 3.14 displays the resistance values considering both AC and DC resistances for each load speed and torque, based on Finite Element Analysis (FEA).

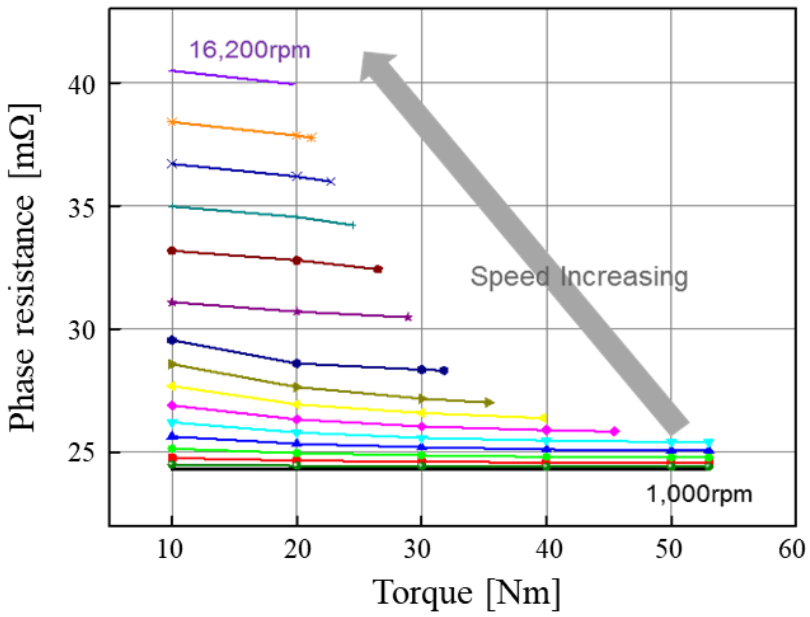
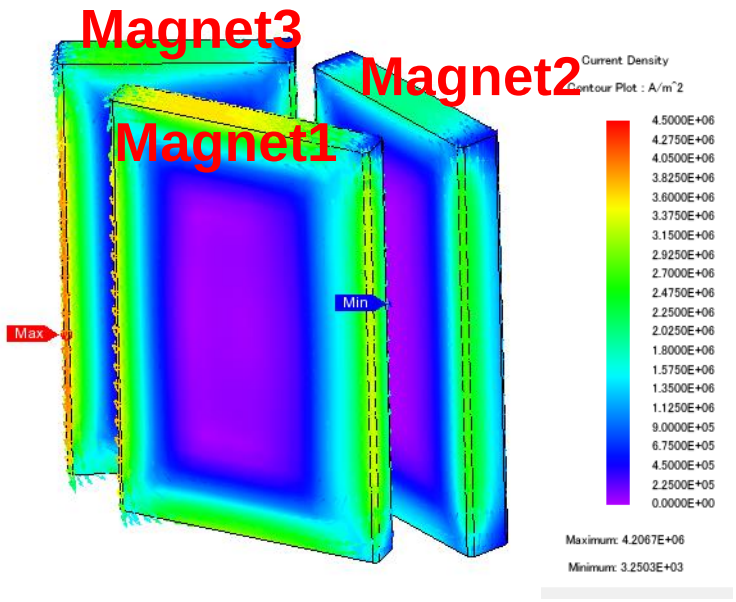
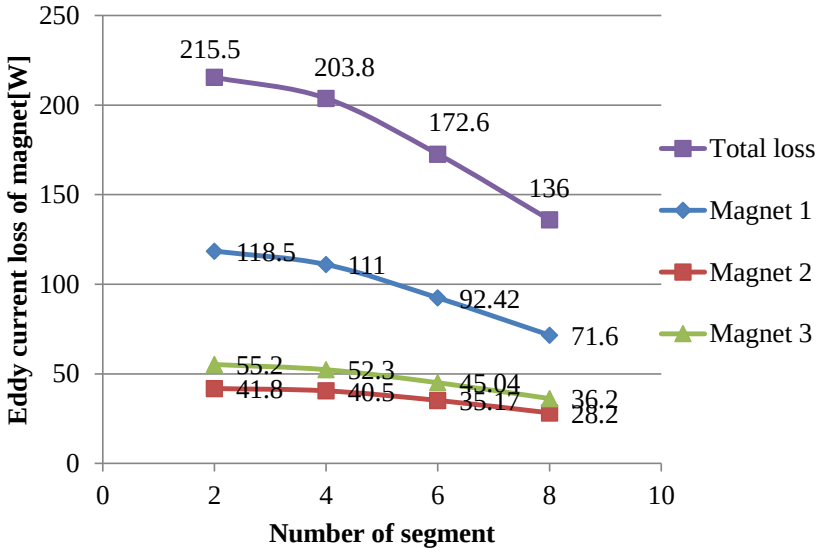


Figure 3.45 Phase resistance depending on the load condition; speed and torque.

The AC resistance increases with a rise in frequency, hence the resistance ascends as the speed elevates. Moreover, as the torque value amplifies, meaning as the load intensifies, the AC resistance slightly diminishes due to the magnetic saturation phenomenon of the surrounding magnetic core.



(a)



(b)

Figure 3.46 (a) Magnet eddy current density in 3D FEA (b) magnet eddy current loss depending on the number of segments.

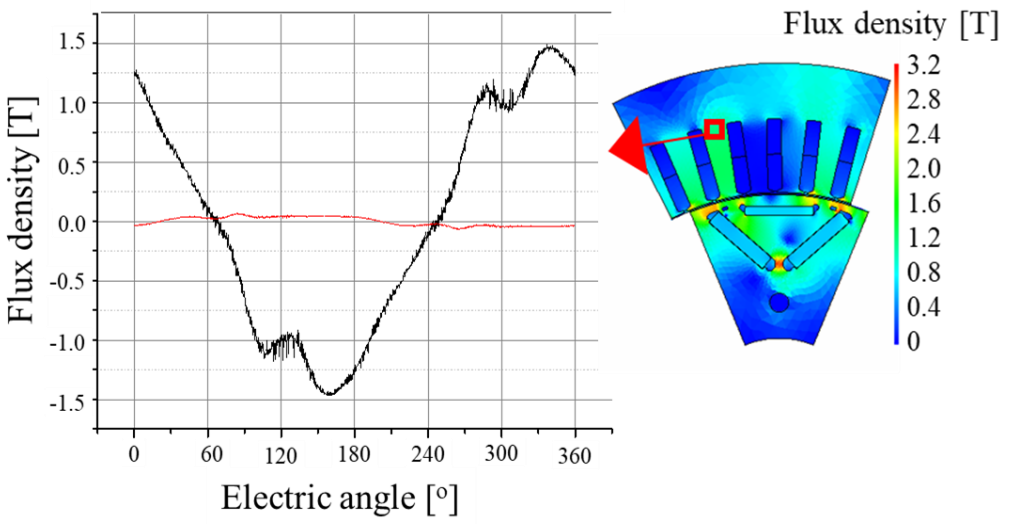
In the case of PMSM, eddy current loss also occurs in the magnet due to changes in the magnetic field. As the current ripple increases, the change in the magnetic field flowing through the magnet increases, so magnet eddy current loss also increases. Figure 3.15 (a) shows the magnet eddy current density distribution obtained by 3D FEA analysis, and as shown in (b), as the segments in the stacking direction are divided, the magnet eddy current loss is reduced.

3.2.5 Iron Loss

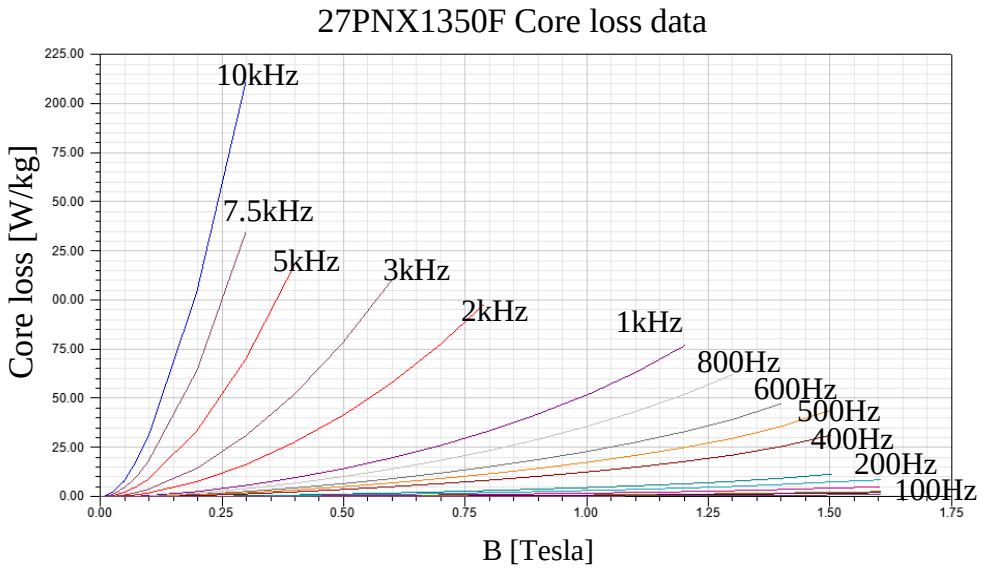
Another significant loss in motors is iron loss, which arises in the magnetic core due to variations in magnetic flux resulting from the current flowing in the magnet and winding. According to the Bertotti formula, iron loss is bifurcated into hysteresis loss, induced by the properties of magnetic materials, and eddy current loss, triggered by fluctuations in magnetic flux [95]. Moreover, there exists an excessive loss term, as illustrated in Equation 3.34. The coefficients C_h, C_e, and C_{ex} represent the hysteresis, eddy current loss, and excessive loss, respectively, and are predicated on the material data of the magnetic core utilized.

$$P_{iron} = P_h + P_e + P_{ex} = C_h f B_m^n + C_e f^2 B_m^2 + C_{ex} f^{1.5} B_m^{1.5} \quad \text{Equation 3.34}$$

In accordance with Equation 3.36, the nonsinusoidal variation in magnetic flux density of each element can be analyzed as harmonic components for each frequency and then applied individually. The total loss is acquired by superposition of the separate harmonic analysis results. Figure 3.16 (a) delineates the alteration in magnetic flux density of the magnetic core based on FEA, and through harmonic analysis, the iron loss can be computed based on the material data in (b).



(a)



(b)

Figure 3.47 (a) Magnetic flux density analyzed by FEA (b) core loss material data

3.3 Summary

In this chapter, drive cycle conditions, foundational to an energy-efficient design of an electric drive system, are examined in depth. A meticulous focus on calculating total loss in most frequently utilized regions of the electric drive, rather than treating whole driving load point, is implemented. This approach is supported by standardized evaluation methods like WLTP and FTP-75, recognized widely in regions such as the US and EU.

These drive cycles are transformed into an electric drive profile by incorporating vehicle dynamics.

To combat potential time and cost inefficiencies in preliminary design stages, an innovative method known as the energy center of gravity method is introduced. This strategy involves calculation of a select few representative points from a multitude of load points, demonstrating an ability to accurately represent the entire cycle, thus improving efficiency, and reducing process complexity.

The overarching design objective to minimize energy consumption requires an in-depth theoretical understanding of the primary losses associated with inverters and motors. Theoretical inverter loss calculations are conducted, aligning with various PWM strategies and device data within a 3L-ANPC, a multilevel inverter topology.

Motor losses are addressed by utilizing the theory of AC Joule loss, iron loss, and magnet eddy current loss, all employing the tool of FEA. This comprehensive understanding and approach facilitate the minimization of losses and progression towards an integrated inverter-motor efficiency design. This energy-centric, holistic approach sets a robust foundation for future advancements in the field of electric drive design.

4 Computer-aided Parametric Inverter-Machine Co-design

This chapter outlines a computer-aided simulation model that enables energy-efficient design and provides an explanation of the methodology. The advanced technology, aimed at minimizing the total energy loss during the drive cycle, to both the inverter and the motor systems.

In terms of the inverter design, to address the high voltage and high-speed requirements of the electric drive, WBG materials such as SiC-MOSFET are utilized. These are combined with a 3L-ANPC topology. The goal is to minimize both switching and conduction losses, as well as the losses associated with the motor during the drive cycle. The selection of an efficient PWM strategy and switching frequency is key to this, and their effectiveness is verified through simulation.

Regarding the motor design, we propose a novel design approach based on the IPMSM model, taking into account the influence of advanced inverter designs using WBG technology. The increased switching frequency made possible by the use of WBG allows for a more flexible and expansive design range in motor parameters such as pole numbers and equivalent series turns. Taking this into consideration, by increasing the number of poles the remarkable energy consumption reduction can be implemented.

A refined co-simulation model is presented for accurately predicting losses in systems applying the latest technology of inverter and motor. Relying on MATLAB SIMULINK simulations, the inverter loss is computed using data-based lookup tables, and output waveforms are simulated. The JMAG-RT model is employed for motor simulations, enhancing the accuracy of loss predictions.

For precise loss calculation in the motor, the commercially available JMAG tool is utilized as a FEA base, which is converted into an RT model and incorporated into the final co-simulation. This simulation methodology bolsters the accuracy of loss predictions.

4.1 Improved 3L-ANPC Inverter Design with WBG

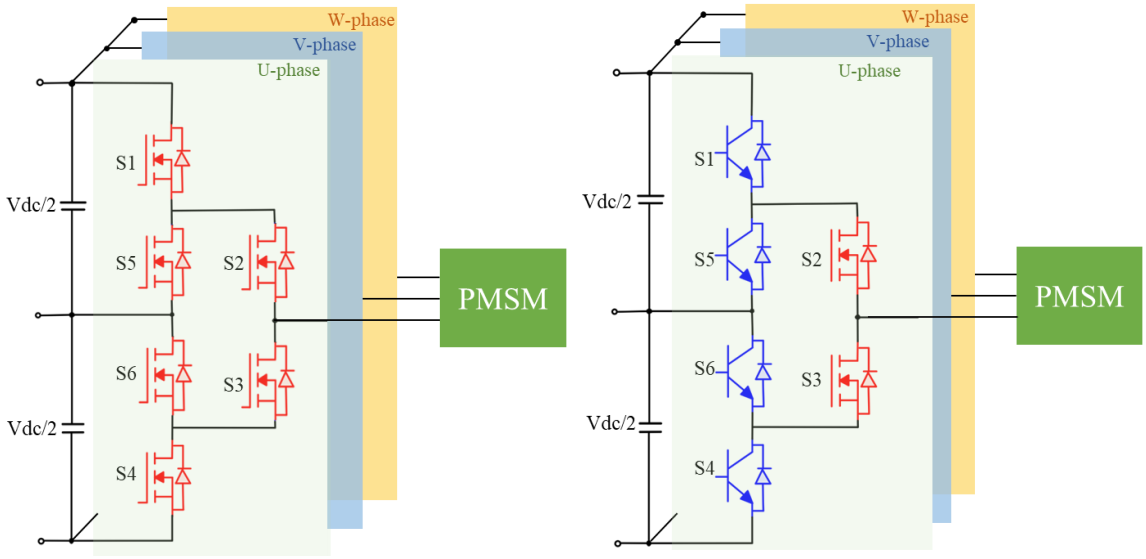
Devices

WBG materials, such as SiC and GaN, have been gaining traction in power electronics due to their superior electrical properties, including high electric field strength, high thermal conductivity, and fast switching capabilities. These characteristics enable WBG-based power devices to operate at higher frequencies, voltages, and temperatures compared to their silicon counterparts, thereby improving overall system efficiency and power density.

The 3L-ANPC topology, on the other hand, offers several advantages such as improved harmonic distortion, lower voltage stress on power devices, and higher output voltage compared to conventional two-level inverters. This results in enhanced system efficiency and reliability, making the 3L-ANPC topology an attractive choice for high-power applications.

In the energy loss reduction design according to the high-speed and high-voltage electric drive, the inverter parameters utilize WBG and consider 3L-ANPC topologies, corresponding PWM, and switching frequency.

4.1.1 3L-ANPC Topologies



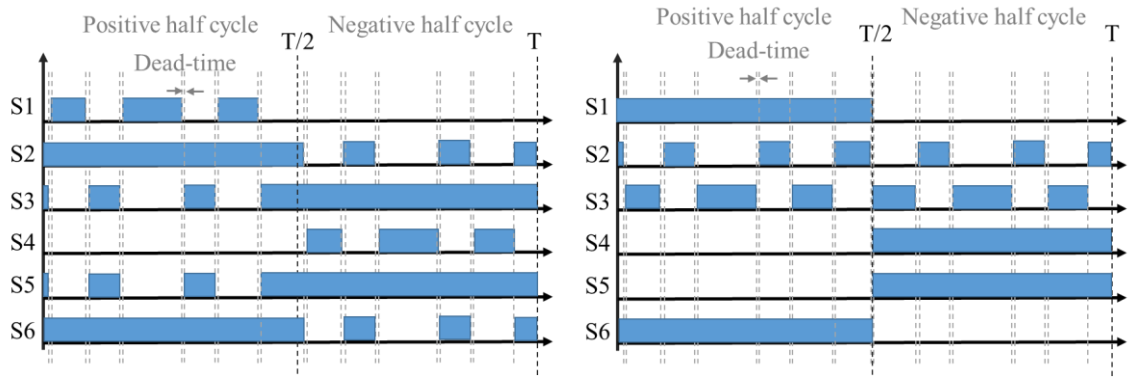
(a) (b)

Figure 4.48. (a) All-SiC 3L-ANPC topology (b) 2SiC-4Si hybrid 3L-ANPC topology

Figure 4.1 presents two 3L-ANPC topologies under consideration in this paper. Figure 4.1 (a) explores the application of SiC-MOSFET devices across all six components within each phase, known as the All-SiC topology. On the other hand, the topology suggested in figure 4.1 (b) is a 2SiC-4Si hybrid topology, where the two components closest to the load utilize SiC while the remaining devices employ Si. As previously reviewed, the employment of SiC can reduce both switching loss and on-resistance, rendering the All-SiC topology generally more advantageous than other hybrid topologies. However, despite significant industrial development, SiC remains pricier than Si-IGBT. In specific PWM strategies, even the implementation of a 2SiC-4Si hybrid topology can offer efficiency reduction akin to that of the All-SiC topology. This indicates that the optimal PWM strategy for loss reduction varies between the two topologies. Therefore, this paper proposes distinct and optimized PWM strategies suitable for each of these topologies.

4.1.2 PWM Strategies

Figure 4.3 illustrates the switching sequence for each state of the two PWM strategies that have been identified to provide optimal loss efficiency when implemented in both topologies. These strategies were initially reviewed in chapters 2.1.3 and 3.2.3.



(a) (b)

Figure 4.49. Two different PWM strategies and switching state (a) LC-PWM (b) LS-PWM

As depicted in Figure 4.2 (a), each switch undertakes high-speed switching in each half-cycle and remains inactive in the remaining half-cycles. The switching action is evenly spread across the six switches, which results in a more balanced distribution of switching loss compared to the Pulse Width Modulation strategy illustrated in Figure 4.2 (b).

Therefore, with an increased switching frequency, this strategy may not be as suitable for the hybrid topology as represented in Figure 4.1 (b). As reviewed earlier, this approach leads to a distributed path for the current flow during the zero state, potentially reducing the conduction loss. Consequently, in the context of this paper, it is referred to as Low Conduction Pulse Width Modulation (LC-PWM).

Table 4.1 presents the switching sequence for each state, taking into account the dead-time for LC-PWM. The switching sequences for O+ and O- are identical, indicating they have a shared zero state. However, distinct sequences are seen during the transitions and for the P and N states, primarily due to the influence of dead-time.

Table 4.9. Switching sequence of LC-PWM strategy

Period	**State**	**Switch**						**Output voltage**
		S1	**S2**	**S3**	**S4**	**S5**	**S6**	
Positive half cycle	P	1	1	0	0	0	1	$+V_{DC}/2$
	P-O^+	0	1	0	0	0	1	0
	O^+	0	1	1	0	1	1	
Negative half cycle	O^-	0	1	1	0	1	1	0
	N-O^-	0	0	1	0	1	0	0
	N	0	0	1	1	1	0	$-V_{DC}/2$

Figure 4.3 illustrates the on/off condition of the switch and the direction of current flow during each state when the PF is set at 1. As depicted in part (a), during the zero state and the dead-time in the positive half-cycle, the current is divided and traverses two paths, specifically S5-S2 and S6-S3. Similarly, in the remaining part of the negative cycle, the current is split between two routes: S2-S5 and S3-S6. Switching losses are greatly influenced by the frequency of device switching. However, as illustrated in Figure 3.9 (a), the energy associated with switching losses increases exponentially, rather than linearly, with rising current. Hence, reducing the current during certain periods could lead to a considerable decrease in switching losses.

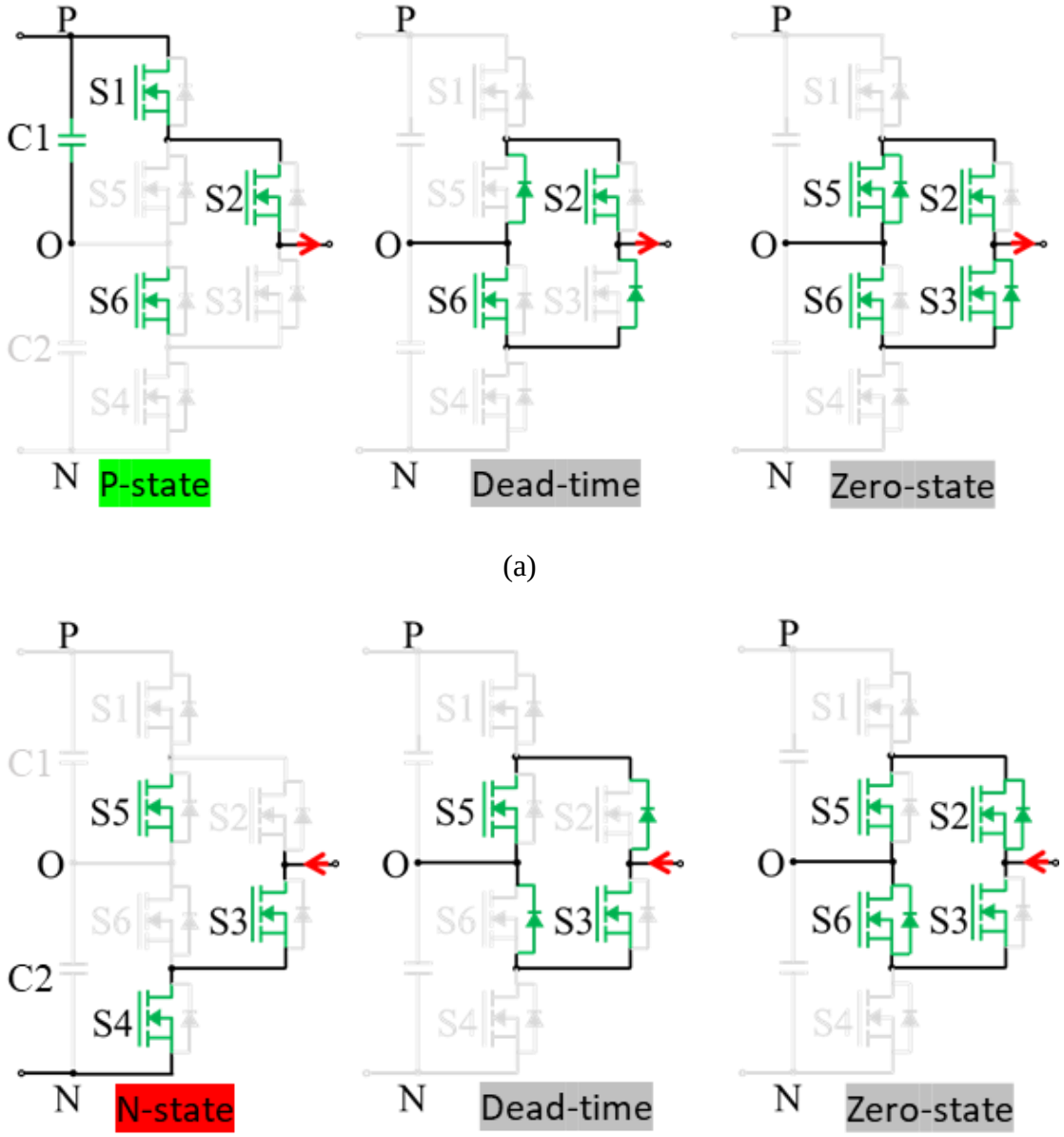


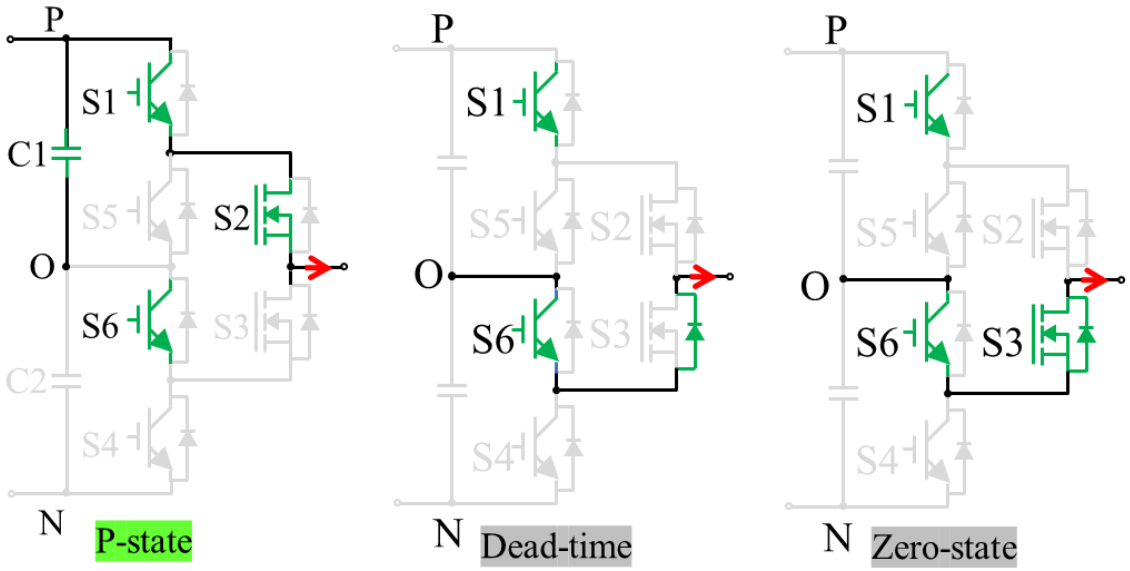
Figure 4.50. Current path and switch state of LC-PWM at (a) positive half-cycle (b) negative half-cycle

Table 4.2 presents an alternative PWM scheme. Throughout the entire cycle, only two devices, S2 and S3, switch at high frequencies, while the remaining devices switch once per half cycle, corresponding to a relatively line frequency. Consequently, this scheme can effectively reduce the overall switching loss. For this reason, it is referred to as the Low Switching PWM (LS-PWM).

Table 4.10. Switching sequence of LS-PWM strategy

Period	State	Switch						Output voltage
		S1	S2	S3	S4	S5	S6	
Positive half cycle	P	1	1	0	0	0	1	$+V_{DC}/2$
	P-O$^+$	1	0	0	0	0	1	0
	O$^+$	1	0	1	0	0	1	
Negative half cycle	O$^-$	0	1	0	1	1	0	0
	N-O$^-$	0	0	0	1	1	0	0
	N	0	0	1	1	1	0	$-V_{DC}/2$

Figure 4.4 similarly demonstrates the current flow and switch state during each stage, under the condition of a PF equal to 1. During the positive half cycle, the current flows through a single path, specifically from S6 to S3, during the dead time and zero state. Conversely, during the remaining cycles, the current follows a path from S2 to S5. In this PWM strategy, only S2 and S3 switches at high frequency, so it is suitable for 2SiC-4Si hybrid topology using both devices as SiC. In an all-SiC topology, effectiveness can be enhanced by substituting these two switches with semiconductors that possess superior switching performance.



(a)

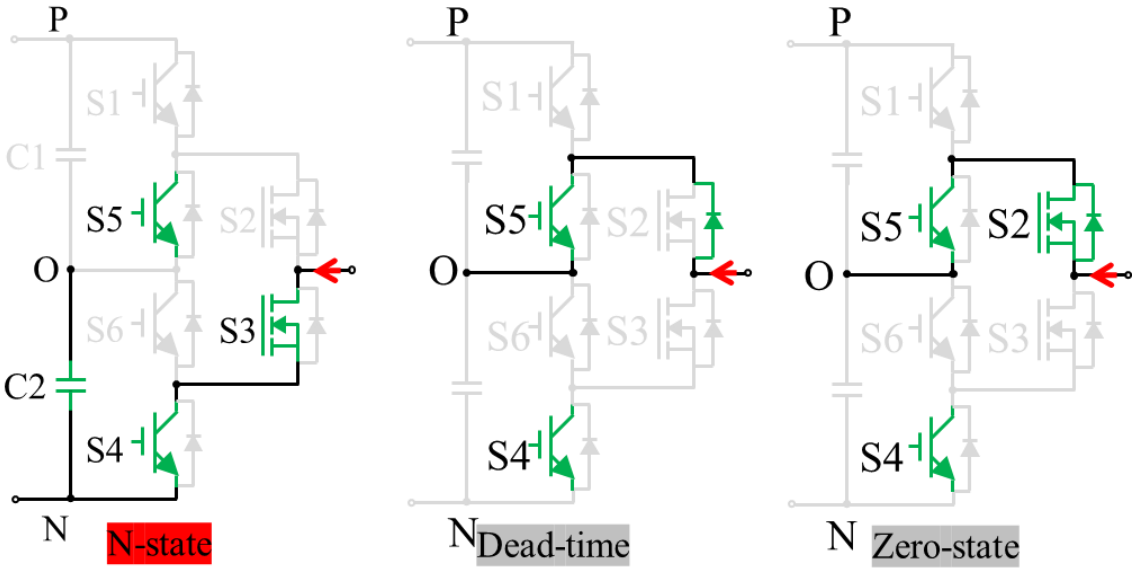


Figure 4.51. Current path and switch state at (a) positive half-cycle (b) negative half-cycle

4.1.3 High Switching Frequency

Elevating the switching frequency augments the switching loss as indicated in Equation 3.22. Hence, purely from an inverter loss perspective, it would be beneficial to adopt as low a frequency as feasible. Nonetheless, a lower switching frequency results in a heightened THD of the output voltage and current, which invariably culminates in escalated losses in the motor. This aspect is particularly prominent as operations exceeding 15,000 rpm are increasing due to high-speed mechanization, and low switching frequencies may fail to regulate desired waveforms at such high speeds. Figure 4.5 presents a comparison of the switching losses between a conventional Si-device and a SiC-MOSFET. WBG devices facilitate designs with elevated overall switching frequencies due to their reduced switching losses. Research is conducted to select an appropriate switching frequency that minimizes the integrated loss of the inverter and machine from a wide range of designable switching frequencies.

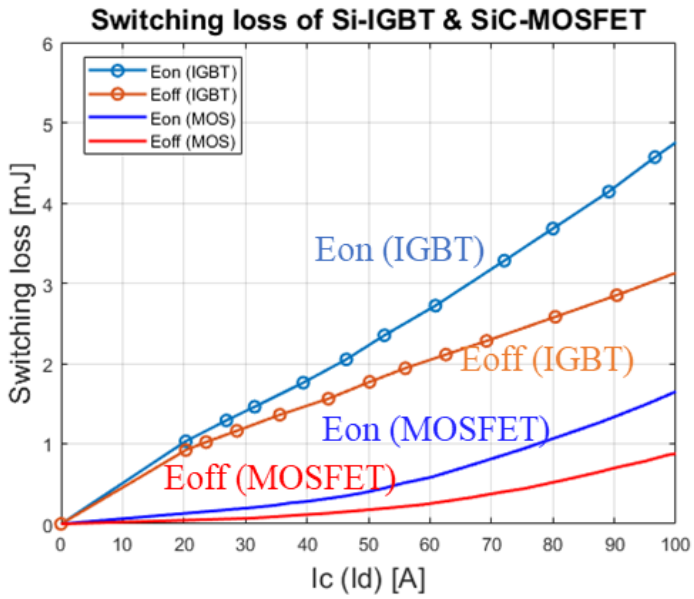


Figure 4.52 Comparison of switching loss for Si-IGBT/diode and SiC-MOSFET

4.2 Novel Design of PMSM

4.2.1 Increasing Pole Number with High Switching Frequency

In motor design, the number of poles n_p is a significant parameter that critically influences performance. Generally, in motor design, the permissible number of poles is largely influenced by the maximum speed of the motor. This is due to the fact that the electrical rotational speed ω_e escalates as the number of poles in the synchronous motor increases, as expressed in Equation 4.1, where ω_m is the mechanical rotational speed.

$$\omega_e = \frac{n_p}{2}\omega_m \qquad \text{Equation 4.35}$$

As the maximum speed of the motor N_{max} increases, the electrical synchronous speed of the motor also increases, which affects the control performance. The maximum number of designable poles is defined as in Equation 4.2, where m_f is the frequency modulation index and f_s is the switching frequency.

$$n_{p\_max} = 120 \times \frac{f_s}{N_{max} \times m_f} \qquad \text{Equation 4.36}$$

Assuming that the minimum m_f for stable control is the same, if the f_s increases, the number of poles that can be designed for the motor under the same maximum speed

requirement increases. An increased number of poles in motor design brings several advantages. One of these advantages is the enhancement of power density.

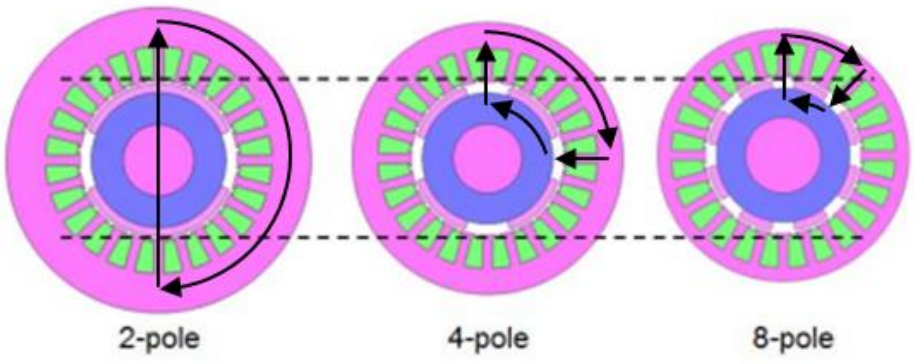


Figure 4.53 Magnetic flux path and yoke thickness depending on the pole number.

As demonstrated in Figure 4.6, increasing the number of motor poles from 2 to 4 and then to 8 can lead to a shortened path of magnetic flux. However, it is essential to highlight that this merely reduces the path, and does not result in an increase in flux due to a reduction in reluctance. Given a constant rotor size, as the number of poles elevates, the flux per pole is inversely proportional to the number of poles' augmentation. Thus, this phenomenon does not lead to an increase in total flux. However, as illustrated in Figure 4.6, a reduction in magnetic flux per pole can contribute to a diminished yoke width. This is tantamount to an enhancement in power density, given that the same output can be achieved with a reduced size. If the same outer diameter of the motor remains constant, the effect of decreasing yoke width, brought about by an increase in the number of poles, can be employed to augment the flux by expanding the outer diameter of the rotor. In [96] and [97], an increase in the number of poles in an axial type of PM motor led to an improvement in power density, and in [98], an increase in the number of poles in an inner rotor type PMSM showed the result of improving efficiency.

Another benefit of increasing the number of poles is the diminishment of DC copper losses. The motor winding features an end-turn section that doesn't contribute to torque. By augmenting the number of poles, the coil pitch distance can be lessened, and coil resistance can be mitigated. This results in a reduction of the overall motor copper loss.

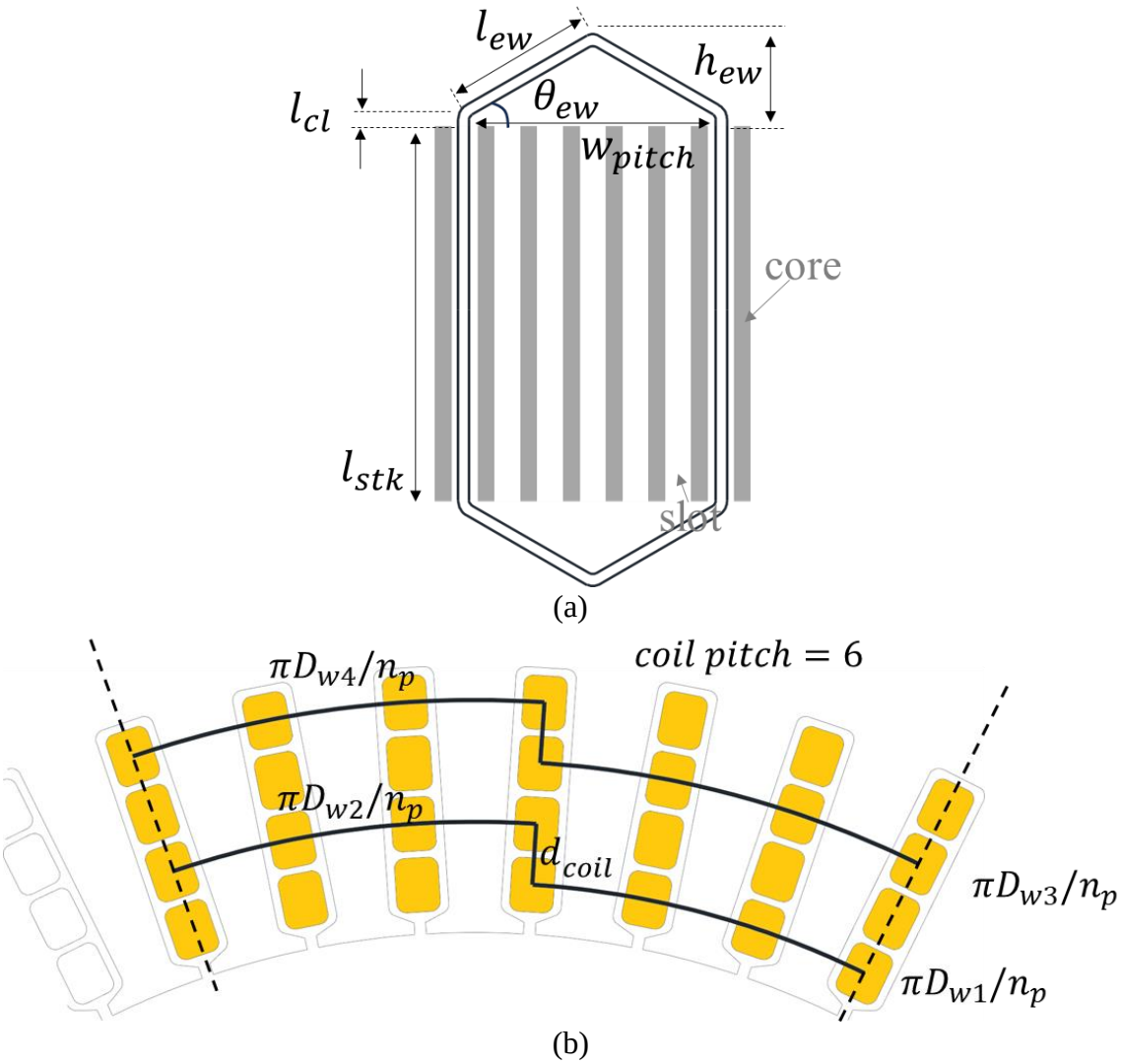


Figure 4.54 Hair-pin winding geometry (a) side view (b) coil pitch width calculation

Figure 4.7 illustrates the geometry of a hair-pin winding. Herein, the DC resistance of the coil R_{DC} can be expressed as Equation 4.3, where l_{stk} denotes stack length, l_{cl} is the clearance length for the manufacturing, l_{ew} is the end-turn length, ρ_{CU} presents resistivity of the coil, A_{coil} and n_T are the cross area of the coil and number of series turn per phase.

$$R_{DC} = \rho_{CU} \frac{2(l_{stk}+2l_{cl}+2l_{ew})}{A_{coil}} n_T \qquad \text{Equation 4.37}$$

$$l_{ew} = \frac{w_{pitch}}{\cos\theta_{ew}} \qquad \text{Equation 4.38}$$

In Equation 4.4, end-turn length is related to the coil pith length w_{pitch} and end-turn angle θ_{ew}.

The angle of the end turn is kept within a certain range to account for stress caused by bending of the hair-pin wire, and when assuming the same angle, it becomes evident that the length of the end turn increases with the pitch length. As depicted in Figure 4.8 (b), given the same size and identical coil pitch, the pitch length shortens as the number of poles increase. Although as the number of poles grows, the diameter in the outer diameter direction of the coil position, such as D_{w1}, D_{w2}, D_{w3}, and D_{w4}, increases, the reduction effect due to the increased number of poles outweighs this. The coil pitch length can be determined using Equation 4.5.

$$W_{pitch} = \frac{\pi(D_{w1}+D_{w2}+D_{w3}+D_{w4})}{2n_p} + d_{coil} \qquad \text{Equation 4.39}$$

This reduction in end-turn length is also observed in other winding types utilizing round wire, not just in the hair-pin configuration.

Presuming an increase in power density due to a decrease in yoke thickness can reduce current for the same size, and considering the effect of reduced end-turns, an assumption that an increase in switching frequency directly leads to an increase in the number of poles can be made. A standardization according to switching frequency is graphically represented in Figure 4.8, illustrating DC copper loss. Theoretically, increasing the switching frequency by 4 times from 5 kHz to 20 kHz enables a DC copper loss reduction close to 60%. However, this value does not account for magnetic core saturation, and AC copper loss and iron loss may rise due to increased electrical speed. Nevertheless, it is evident that the motor design range has been expanded with this increase in switching frequency, which enables the design of a machine with reduced energy loss.

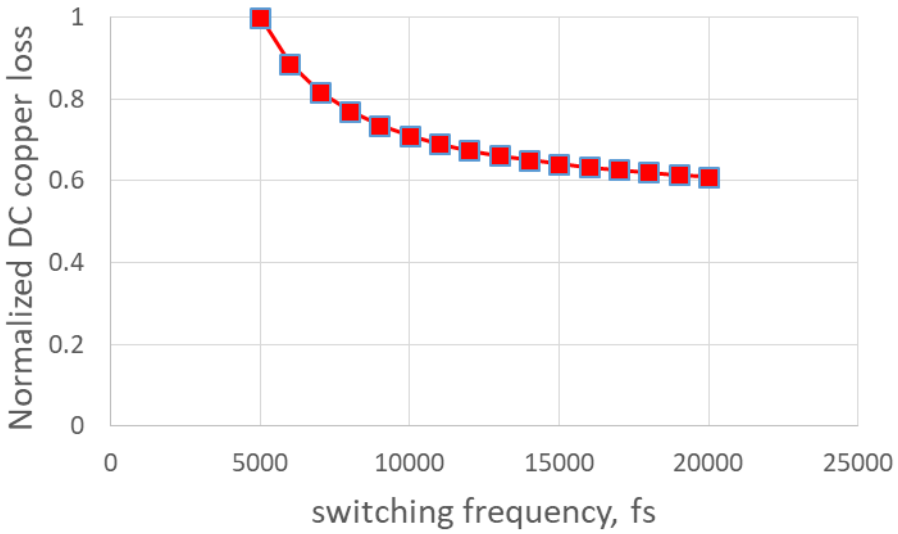


Figure 4.55 Theoretical calculation of normalized DC copper loss as per switching frequency.

4.2.2 Inductance Design Considering Co-effect

The THD of the inverter output is influenced not only by the switching frequency but also by the voltage level and PWM strategy. Another significant factor is the inductance value of the motor. Lower inductance values can elevate current harmonics under identical conditions, resulting in increased motor losses. The inductance value of the motor can be defined by Equation 4.6 [99], where μ_0 is the magnetic vacuum permeability, k_c is the carter coefficient, g denotes the airgap length, and k_{w1} is the winding factor. Generally, inductance is directly proportional to the square of the number of turns.

$$L = \frac{3\mu_0 D_r l_{stk}}{\pi \cdot n_p^2 \cdot k_c \cdot g} (k_{w1} \cdot n_T)^2 \qquad \text{Equation 4.40}$$

Inductance is a crucial factor influencing motor torque, and ensuring output quality through high switching frequency implies that the design flexibility of inductance also improves. The optimal value of equivalent series turns, which influences motor inductance, can be theoretically calculated as depicted in Equation 4.7. Here, P_{max} is the maximum power in base speed, and B_g represents the air gap flux density.

$$n_T = \frac{P_{max}}{3 i_{s\_max}} \cdot \frac{\sqrt{2}}{\pi^2} \cdot \frac{60}{\omega_m k_{w1} B_g D_r l_{stk}} \qquad \text{Equation 4.41}$$

A notable limitation of hair-pin winding lies in its design, which only permits even number of layers due to the process of inserting a pre-fabricated hairpin coil rather than winding directly [100]. This factor restricts the number of equivalent series turns that can be designed compared to general circular distribution winding. It is influenced by the pole-slot combination. As stated earlier, if pole number selection is freely permitted, the designer's choice of the number of equivalent series turns is broader even in the combination of the same pole and slot numbers in hairpin type.

Ultimately, due to the impact of WBG on the motor, the design range of motor pole numbers and equivalent series turns, which form the basis of the design, broadens, leading to substantial reduction in the energy loss of the entire system. By considering both the inverter and these broader motor parameters, an energy efficient electric drive design is proposed.

4.3 Co-simulation Model

Here outlines a computer-aided simulation model that enables energy-efficient design and provides an explanation of the methodology. Utilizing MATLAB Simulink, this approach allows for in-depth analysis of inverter topology and power devices, covering aspects such as loss analysis and electrical characteristics.

Figure 4.9 presents a general schematic of the complete co-simulation model. For the energy efficiency outlined in the previous chapter, the inverter model is primarily constructed using 3L-ANPC topology and WBG devices as ① in Figure 4.9. Concurrently, the motor model, designed mainly to meet basic performance requirements, is analyzed based on FEA with JMAG Designer. Analysis of the model, through the determined motor design parameters, yields L_d, L_q, Ψ_m, V_{LL}, and motor loss including Joule, iron and magnet eddy current loss according to I_a, β, and ω_e. Here, L_d and L_q are motor d, q-axis inductance, Ψ_m is the magnet flux, V_{LL} is the line-to-line voltage. Additionally, I_a, β, and ω_e are the phase current, beta angle, and electrical rotational speed. These values are provided in the form of a map. From this map information, the most efficient reference d-axis current $i_{d\,ref}$, q-axis current $i_{q\,ref}$ can be calculated. Now, under the operating point condition, which is the main target, the above motor output parameters are analyzed

together with the inverter. At this time, the motor model uses the PMSM model of MATLAB Simulink like as ②. The difference between this model and the RT model will be explained in detail later. As shown in ③, the current control logic of the inverter receives rotational speed, position, voltage, and phase current values from the PMSM model as feed-back closed loop control, and performs current control to create reference current using general PI-control as presented in ④ [101]. In this case, constant rotor speed condition is used. The various PWM strategies of 3L-ANPC to make the reference voltage obtained from the PI-control part are composed in ⑤. ⑥ illustrates the RT model used in the final stage of loss analysis, utilizing the model designed as an integrated system. During this process, motor parameters such as L_d and L_q are not static values at a specific load condition, but instead of fluctuating based on the mechanical angle.

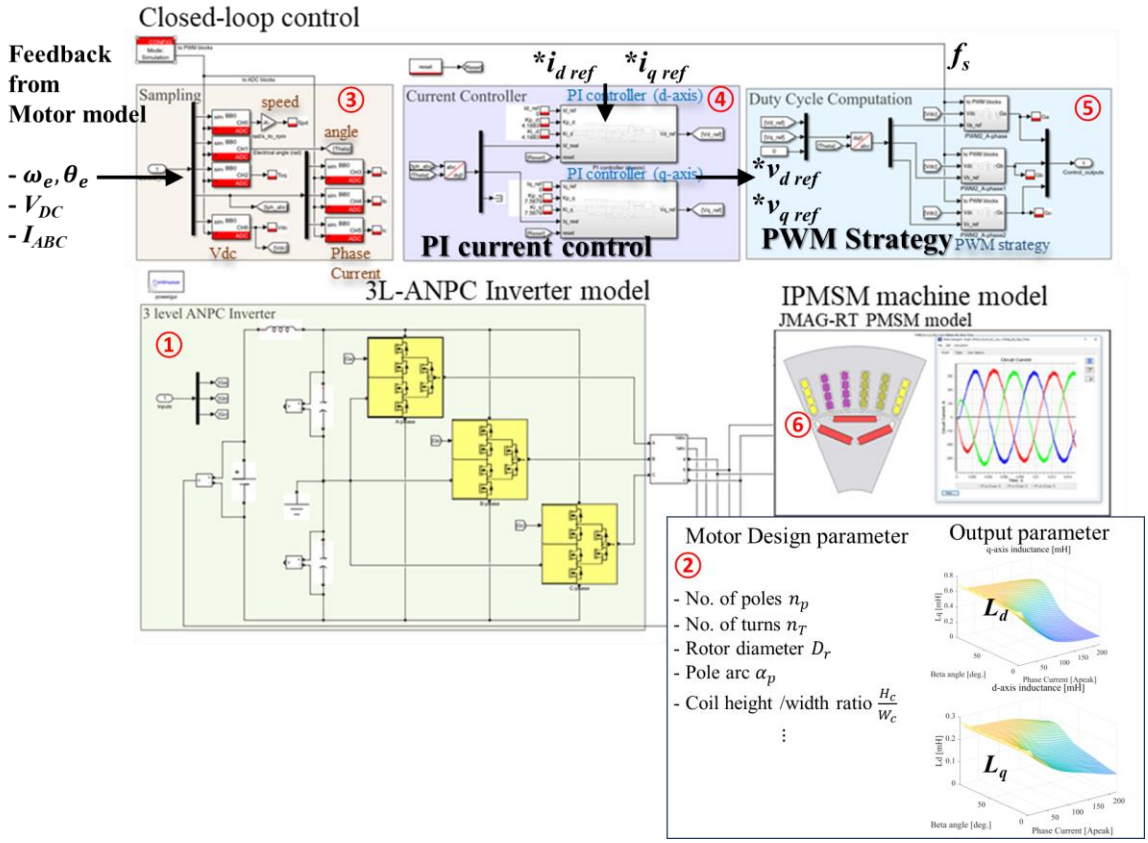


Figure 4.56 Co-simulation model for evaluating design.

4.3.1 Inverter Functional Model

The topology depicted in Figure 4.1 is formulated utilizing MOSFET and IGBT SPICE models from MATLAB Simulink [102]. Device data is set up via tabulated data as demonstrated in Figure 4.5. On Simulink, load can be set using R-L, a passive element, or through the Simulink PMSM model or JMAG-RT model. For the preliminary design, the PMSM model with motor parameters fixed at certain points is used, and lastly, the JMAG-RT model is introduced to enhance the accuracy of the loss calculation.

Figure 4.10 illustrates the conduction loss and switching loss model of the inverter's power device component. The conduction loss and switching loss are computed in accordance with the PWM strategy using a Look-Up Table (LUT) created from the datasheet. A gate signal can be generated in the PWM strategy, and the voltage and current state of each switching device can be simulated correspondingly. The switching loss (indicated by the blue box in Figure 4.10) and conduction loss (marked by the green box in Figure 4.10) are computed using the LUT with the voltage and current data of the simulated device as input. The calculated switching energy from the LUT is converted into power in watts by determining the turn on / turn off timing. The conduction loss is calculated using the V-I characteristic curve data LUT.

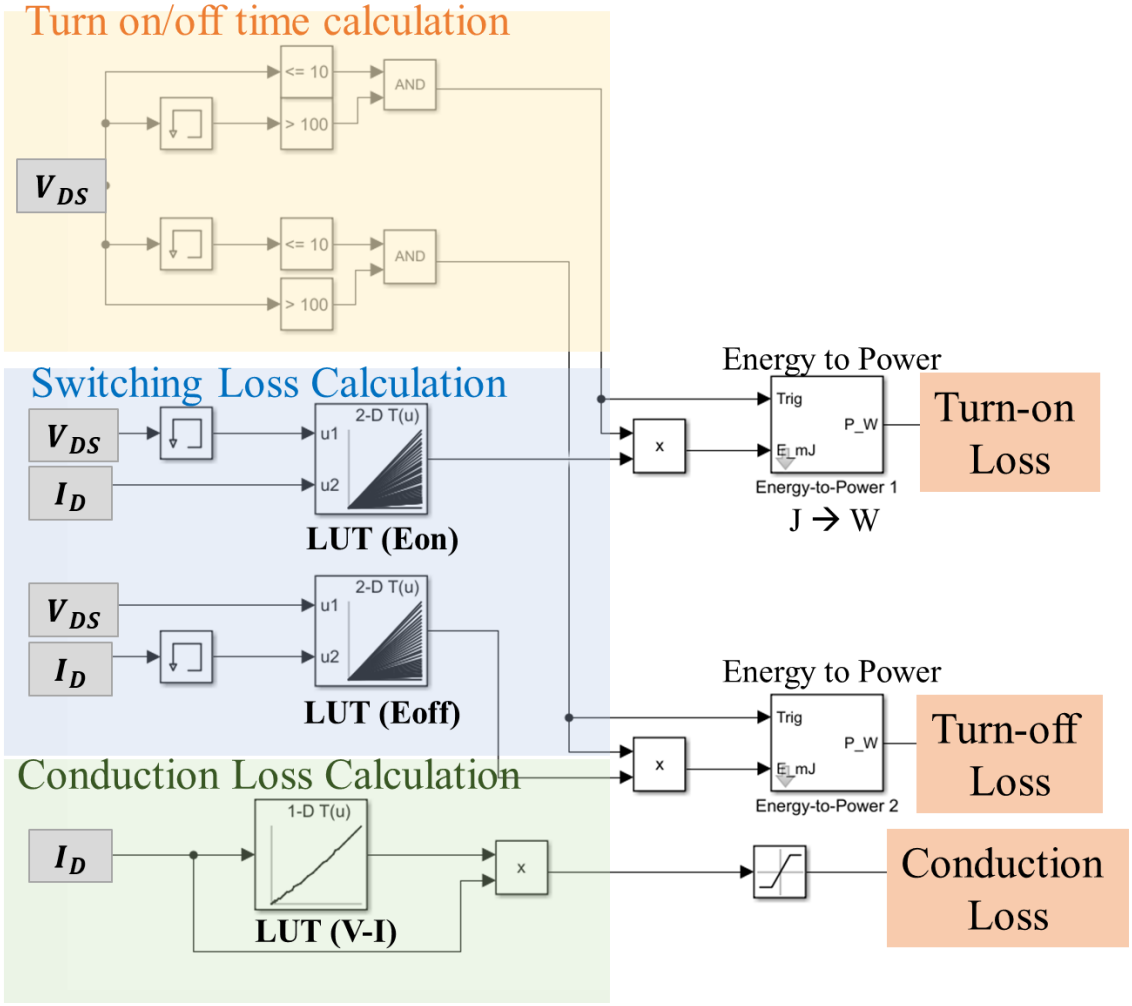
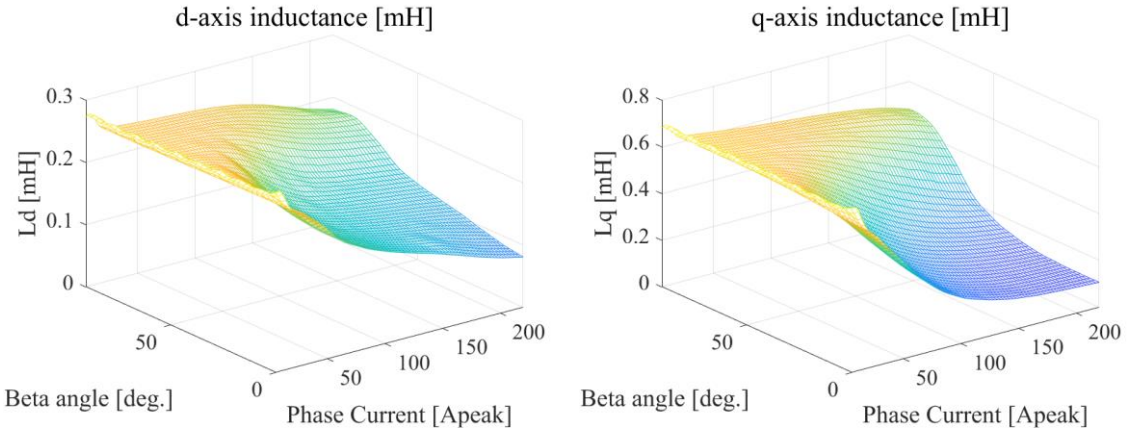


Figure 4.57 Inverter switching and conduction loss calculation model.

4.3.2 FEA Based PMSM Model

The initial design of the number of poles and turns of the motor is performed based on the IPMSM model, and at this time, the current waveform extracted from the inverter simulation is used as input. The modeling process involves the use of JMAG Designer, a FEA based tool, for the machine model analysis. JMAG Designer allows for meticulous examination of electromagnetic fields, delivering a thorough understanding of the motor's behavior under varying conditions. This precision enhances the prediction and optimization of machine performance, thus leading to improved energy efficiency. The machine model from JMAG Designer is then integrated with the inverter model on Simulink, achieved via the JMAG-RT model [103-105]. JMAG-RT offers a bridge

between detailed FEA models and system-level simulations on Simulink, thereby enabling concurrent examination of power devices and the machine. It translates the intricate FEA models into equivalent circuit models that can be readily used in Simulink for systems simulation. This interconnected approach allows a comprehensive analysis of both machine and power electronics as a complete system, offering insights into their interdependencies and overall system performance. It provides a holistic view of the system design, leading to enhanced optimization strategies for energy efficiency. This method of computer-aided design not only reduces the need for physical prototypes but also accelerates the design process, enabling rapid and efficient exploration of design alternatives.

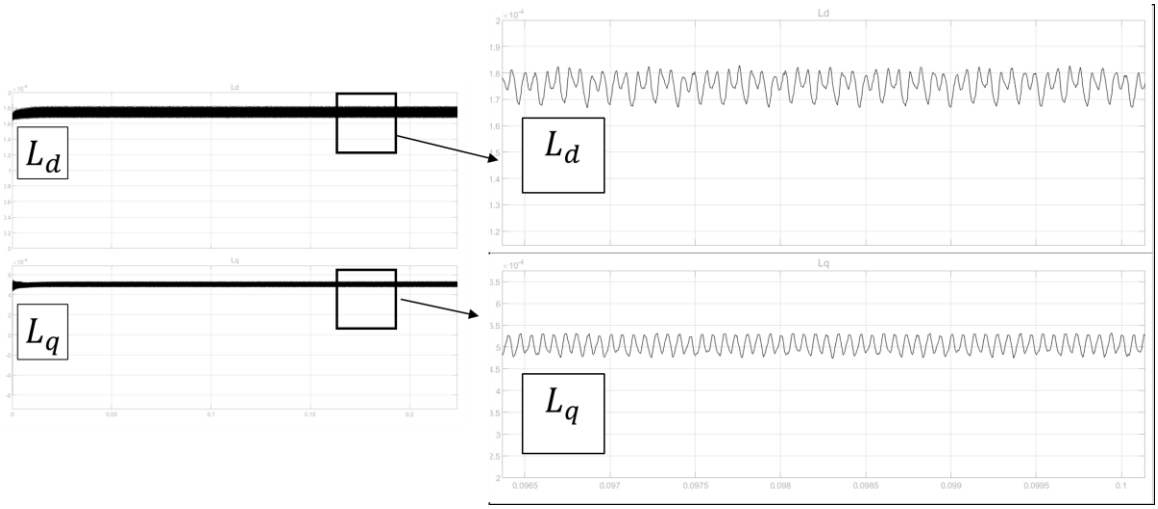


(a) (b)

Figure 4.58 Inductance map of the motor depending on i_a and β in (a) d-axis L_d (b) q-axis L_q.

Figure 4.11 displays the L_d and L_q map, which can be derived by simulating the motor model's total current and beta angle. Besides these, various output parameters such as voltage and loss can also be calculated. As previously mentioned, parameters like L_d and L_q are assumed to be constant when the current and beta angle are determined through maximum efficiency control. This assumption is made to simplify control as these values, although they vary with the rotor's angle, are converted into a fixed DC value through d-q axis conversion. However, in reality, even with d-q axis conversion, these parameters vary with the rotor's rotational angle as the waveforms are not ideally sinusoidal. In the JMAG-RT model, these output parameters have values that change not only based on the phase

current i_a and β but also the motor position, an additional variable. As depicted in Figure 4.12, the values of L_d and L_q minutely change depending on the motor's rotational state, and the difference amplifies when the saturation is severe.



(a) (b)

Figure 4.59 Inductance variation depending on rotor position simulated by using JMAG-RT model.

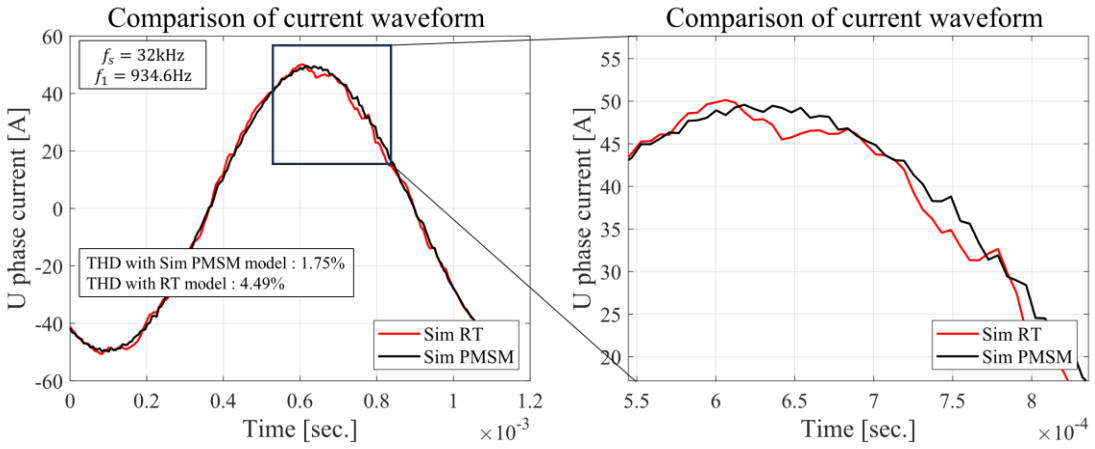


Figure 4.60 Comparison of the output current waveform (U-phase current) between the simulated by JMAG-RT model and Sim PMSM model.

More accurate model predictions can be made by accounting for parameters that change in real-time with the rotor's position. Figure 4.13 shows the results of an inverter-motor coupled simulation using a JMAG-RT model, which varies with the rotor position, and a Sim PMSM model that uses a fixed value. Differences in some current waveforms

can be observed due to differences in inductance at the current peak section. The simulation results indicate that the difference in THD increases from 1.75% to 4.49% when reflected in the RT model. This discrepancy tends to increase as the current value rises.

In this way, the accuracy of the analysis can be improved by considering parameters that change according to the rotor position.

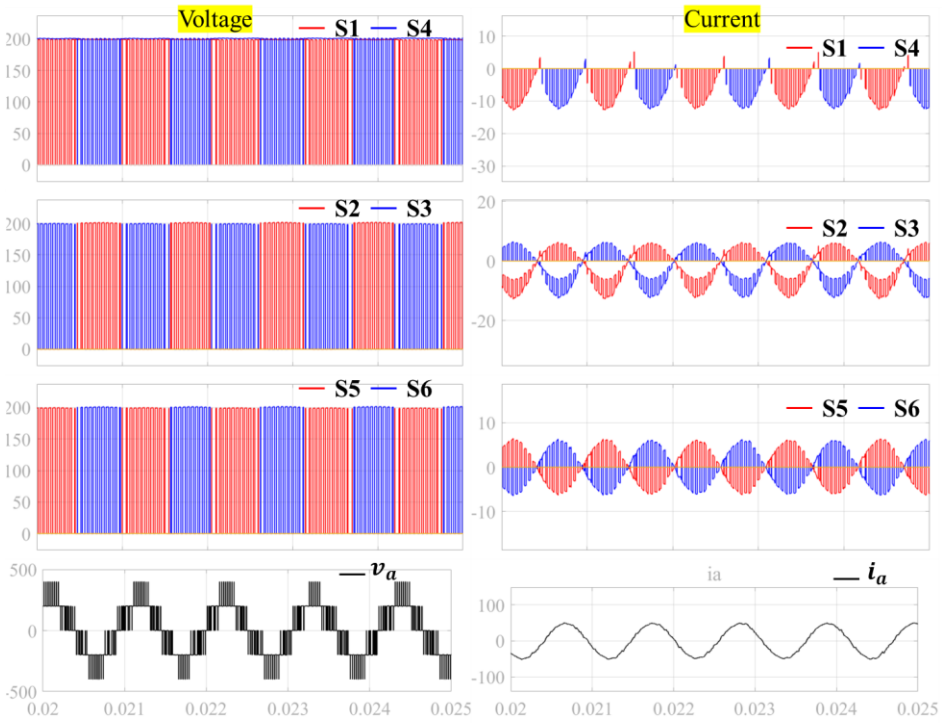
4.3.3 Simulation Results with Co-simulation Model

Table 4.3 displays the PWM strategy employed with this model, as well as the conditions for reviewing simulation results based on the switching frequency. The motor model utilizes the enhanced 400V model from Chapter 5.1, with the model's geometry demonstrated on the right side of Figure 5.8.

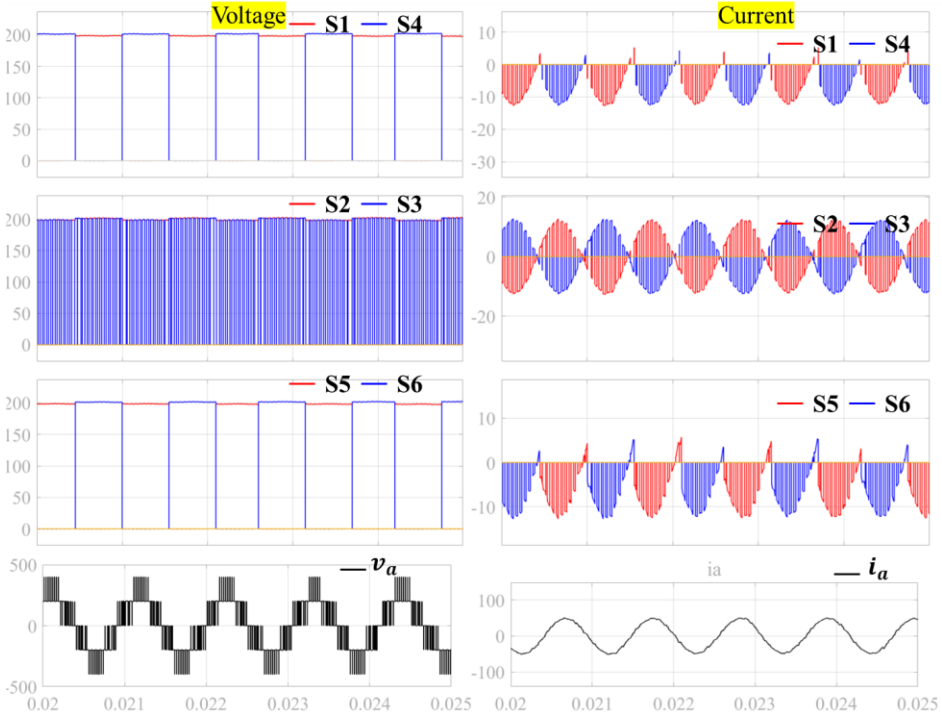
Table 4.11. Simulation conditions

Inverter	PWM	f_s [kHz]	Speed [rpm]	Torque [Nm]
3L-ANPC All-SiC	LC-PWM	20	11,215.9	-11.9
		40		
	LS-PWM	20		
		40		

Figure 4.14 presents the voltage and current state for each switching devices, as well as the U-phase output waveform, corresponding to the two PWM strategies at a switching frequency of 20kHz. Under the corresponding speed and torque conditions, power generation conditions are exhibited, and the two PWMs are regulated to approximately PF=-0.97. With the LC-PWM condition, since the current in the 0 state is allocated across two paths, S2-S5 and S3-S6, it can be observed that the current load for the four devices is evenly distributed over the entire cycle. For LS-PWM, there is a benefit in that switching scarcely occurs for devices apart from S2-S3. As depicted in Figure 4.15, LS-PWM exhibits a concentration of loss in S2-S3, and with an increase in the switching frequency, it appears more advantageous than LC-PWM in reducing overall switching loss. However, the outcome depends on the load condition, specifically, the magnitude of voltage and current. This will be discussed in detail in Chapter 5.



(a)



(b)

Figure 4.61 Simulation results: voltage and current for each power device and output load (a) $f_s = 20kHz$, LC-PWM (b) $f_s = 20kHz$, LS-PWM.

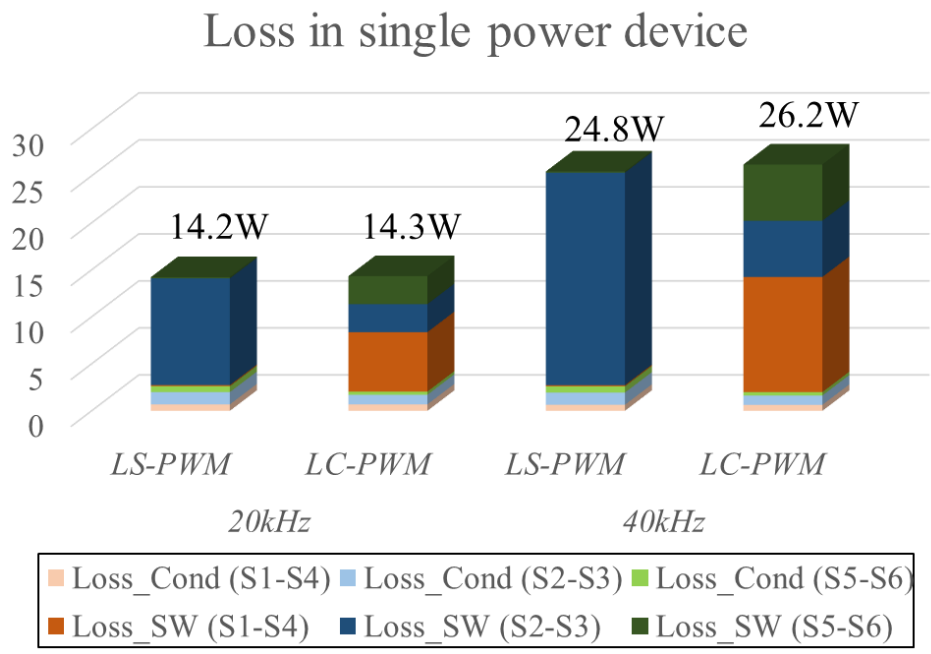


Figure 4.62 Simulation results: power device loss in single device depending on the PWM strategies and switching frequencies.

4.4 Summary

This chapter detailed design approaches regarding inverters and motors for enhancing energy efficiency. With respect to inverters, the application of two topologies - 3L-ANPC and the idea of incorporating WBG devices - were examined, as well as the PWM strategy which would vary dependent on load condition. Additionally, switching frequency emerged as a crucial parameter in minimizing total system energy loss.

For motor design, the usage of WBG devices and the increased freedom in designing the number of poles and turns, afforded by the 3L-ANPC topology, were elucidated. An increase in switching frequency allows for an increased number of poles for the same motor specification, and also extends the design limit for the number of turns. An approach for achieving energy improvement in a motor was presented based on these insights.

Furthermore, a simulation model designed for predicting the entire system's energy loss was outlined. The co-simulation model of the FEA based motor model with the Simulink-based inverter model amplifies the accuracy of the entire system's loss prediction.

5 Case Study-based Simulation Results

In this chapter, based on the design methodology explained so far, the results of enhancing existing benchmark designs in terms of energy loss during the drive cycle are shown, through simulations that reflect actual EV systems. advanced design methods and outcomes for 1) the P0 application in a 400V system of a PHEV, and 2) the traction application in an 800V system of a BEV are presented. The inverter utilizes WBG material, SiC-MOSFET, and employs a 3L-ANPC topology to enhance switching frequency and overall output waveform quality. Two different topologies and corresponding PWM strategies are deeply discussed with some simulation results. For the machine design, leveraging the results from the improved inverter design, s more efficient machine design based on IPMSM is proposed. Focusing on the drive cycle described in Chapter 3.1 for the US and EU, the primary operating points are extracted, and these are employed for energy efficient design. The design proceeds accordingly, total driving energy loss is compared, and the improved energy efficient system is presented. In addition, a hybrid PWM strategy, which uses a combination of two PWM strategies depending on the load point, is also explained.

5.1 Case Study A: 400V B-ISG System for PHEV

PHEVs utilize two power sources, a traditional internal combustion engine and an electric motor, to drive the vehicle. Unlike Mild hybrid, PHEV has a separate external charging system, and there is an electric drive mode driven only by an electric motor. In the transition to BEVs, PHEVs remain attractive and can be an alternative, especially in countries with insufficient electric charging infrastructure [1]. The design topology of a PHEV, dictated by the positioning of the motor relative to the internal combustion engine and the wheels, greatly influences the performance, efficiency, and overall characteristics of the vehicle. PHEVs are typically categorized into five systems based on this motor placement: P0, P1, P2, P3, and P4 [106]. Figure 5.1 shows layout categories according to the location of the electric machine in the hybrid electric vehicle. P0 is a B-ISG system connected by a belt to the engine's rotating shaft pulley. It serves as a starter motor that starts the engine and a generator that charges a low-voltage battery such as a 12V battery

from the driving force of the engine. The ISG replaces these two and integrates them into one machine. It's predominantly utilized in mild hybrid systems. This configuration enables improved fuel economy with minimal changes to the vehicle's system topology. Therefore, the 48V system B-ISG has been researched extensively and applied in numerous vehicles [107].

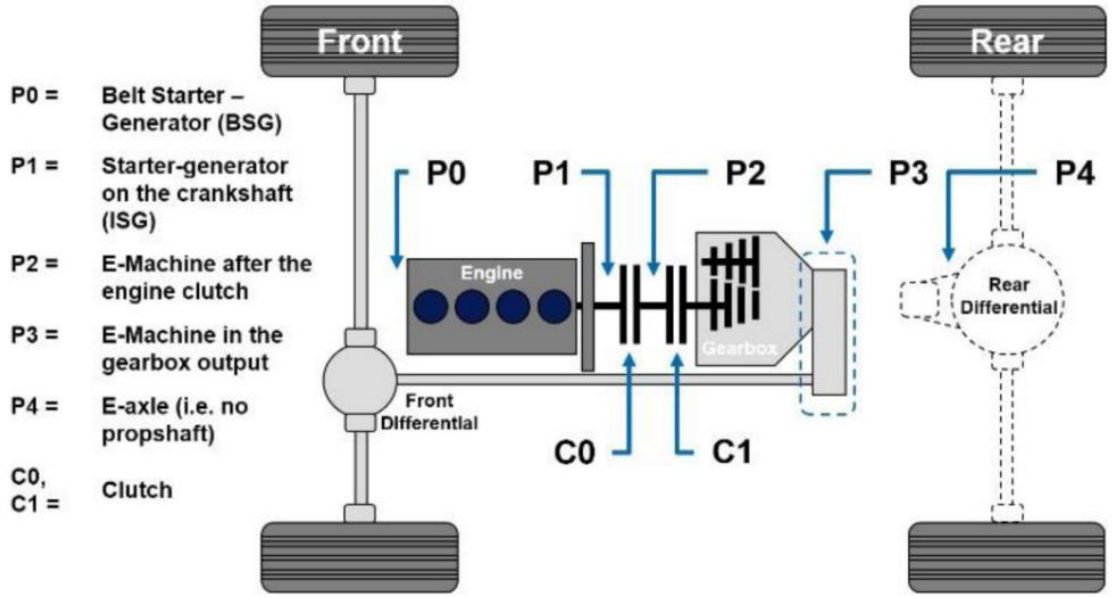


Figure 5.63 System diagram of the electric machine positions in hybrid electric vehicle, from [106].

The High voltage ISG system applies the same role as the 48V B-ISG to high voltage PHEVs, such as those in a 400V system, but expands its function beyond merely starting the engine and serving as an alternator. As it advances into high-voltage specifications, motors such as claw-pole types have been developed into PM machines like IPMSMs, as referred in [107]. As the B-ISG operates within the confined space of the engine compartment, a compact design is critical. While its operation speed can vary based on the pulley ratio with the engine shaft, it generally operates at high speeds. Furthermore, despite its relatively small size, it is driven at a comparatively high voltage for its size, such as 400V, leading to various design challenges. Given the restricted stack length, usage of magnets, and high maximum rotational speed, the inductance of the motor is relatively small, as shown in Equation 4.6. However, because of high voltage driving such as 400V,

the current THD becomes large even at the same switching frequency, which can lead to significant losses in the motor. Additionally, because it operates in a high-temperature engine compartment, thermal design considerations for high temperatures are also crucial. Therefore, despite the increase in costs, it is possible to address these challenges through the use of topologies such as WBG and 3L-ANPC, along with the accompanying improved design. This approach can enhance the energy efficiency of the entire PHEV system.

5.1.1 Benchmark Design

Table 5.1 presents specifications for existing benchmark specifications. The maximum output is 30kW, the peak torque for engine start-up is 50Nm even under cold-start conditions, and the maximum speed goes up to 18,000rpm, taking into account the 3:1 pulley ratio. The inverter design is a two-level, three-phase inverter using conventional Si-IGBT devices, and the switching frequency is limited to 10kHz due to the use of IGBT. The machine design is an 8-pole, 48-slot, hair-pin type IPMSM.

Table 5.12. Benchmark 400V B-ISG system specification.

Item		**Specification**
Peak power		30kW (motoring & generating)
Peak torque		±50Nm
DC-link voltage / max. phase current		400Vdc / 180Arms
Max. ratating speed		18,000 rpm (3:1 pulley ratio)
Inverter	Inverter topology	Si-IGBT 2L 3phase Inverter
	Switching frequency	10kHz
Machine	Machine type	IPMSM (NdFeB magnet)
	Pole / slot	8/48
	Outer diameter / stack length	130mm / 55mm
	Winding type	Rectangular hair-pin winding

Figure 5.2 displays the load points for the B-ISG profile of the hybrid vehicle derived from the US 06 drive cycle. The ten primary points, which are obtained from the energy gravity center method as described in Chapter 3.1.3, are also illustrated in Figure 5.2 (b). The specific torque and speed values of these load points are provided in Table 5.2. Based on this main point, The model in Chapter 4 is used to analyze the loss and proceed with improvement design.

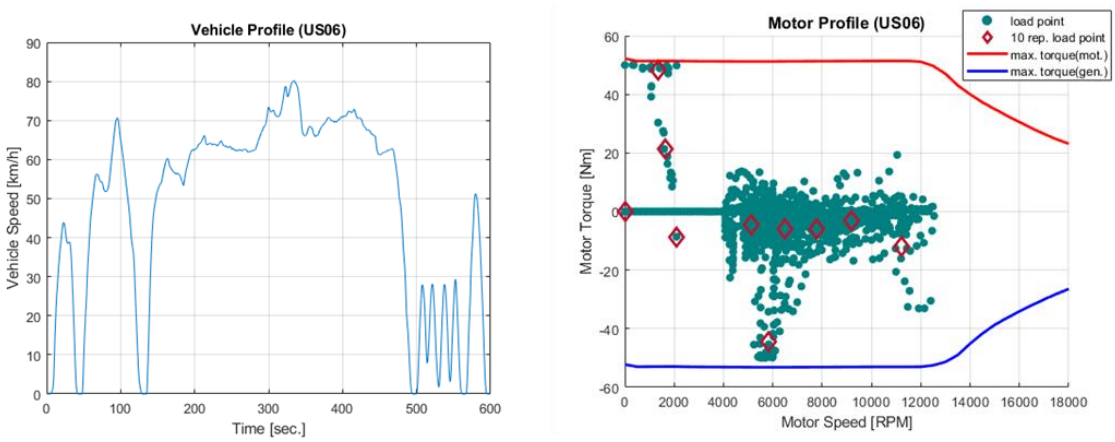


Figure 5.64 Drive cycle profile (a) vehicle profile (US06) (b) machine profile

Table 5.13. Representative load point from energy gravity center method.

No.	Time[sec.]	Speed [rpm]	Torque [Nm]
1	1.2	1640.9	21.2
2	2.7	1342.4	48.3
3	8.6	5815.1	-44.5
4	12.9	11215.9	-11.9
5	22.4	2094.8	-8.6
6	36.6	9186.7	-3.3
7	42.0	7789.6	-5.9
8	77.9	6490.6	-6.0
9	195.0	5105.2	-4.5

5.1.2 Improve Design

Inverter design considers both All-SiC and 2SiC-4Si hybrid topologies in Figure 4.?. The power device model used for the 3L-ANPC inverter and 2level inverter are represented in the Table 5.3. Additionally, the V-I characteristics and switching loss for the 650V class SiC MOSFET and the 600V class Si-IGBT used in the 3L-ANPC are illustrated in the Figure 5.3. Using the data in Figure 5.3 (a), conduction loss can be calculated with the help of a look-up table, and switching loss can be derived from the data in Figure 5.3 (b).

Table 5.14. Power device specification for 2L and 3L-ANPC.

Topology	Device	Part No.	V_{ce} / V_{ds}	I_c / I_d	Remarks
2L-HB	Si-IGBT/Diode	Infineon - IKQ75N120CT2	1200	75	3-parallel
3L-ANPC	Si-IGBT/Diode	Infineon – AIKQ120N60CT	600	120	2-parallel
3	SiC-MOSFET	Wolfspeed - C3M0015065D	650	120	2-parallel

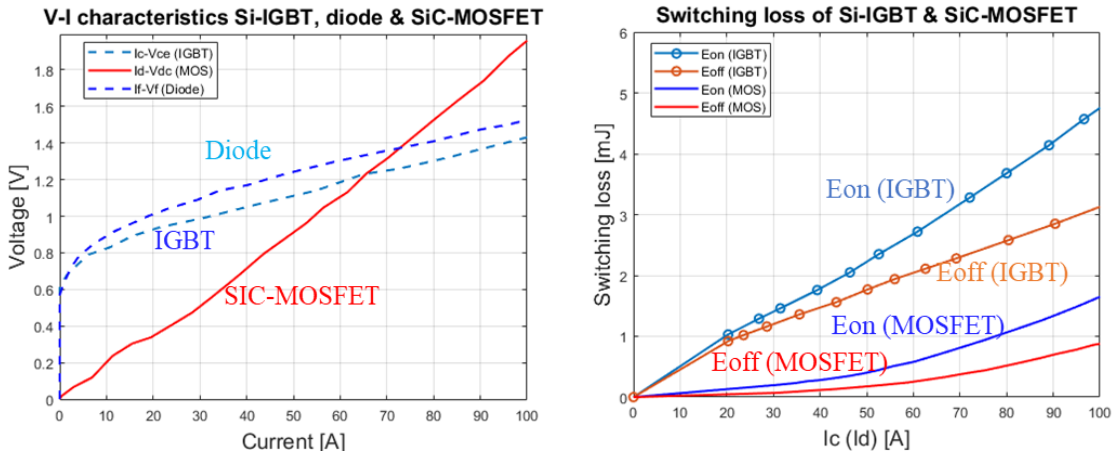
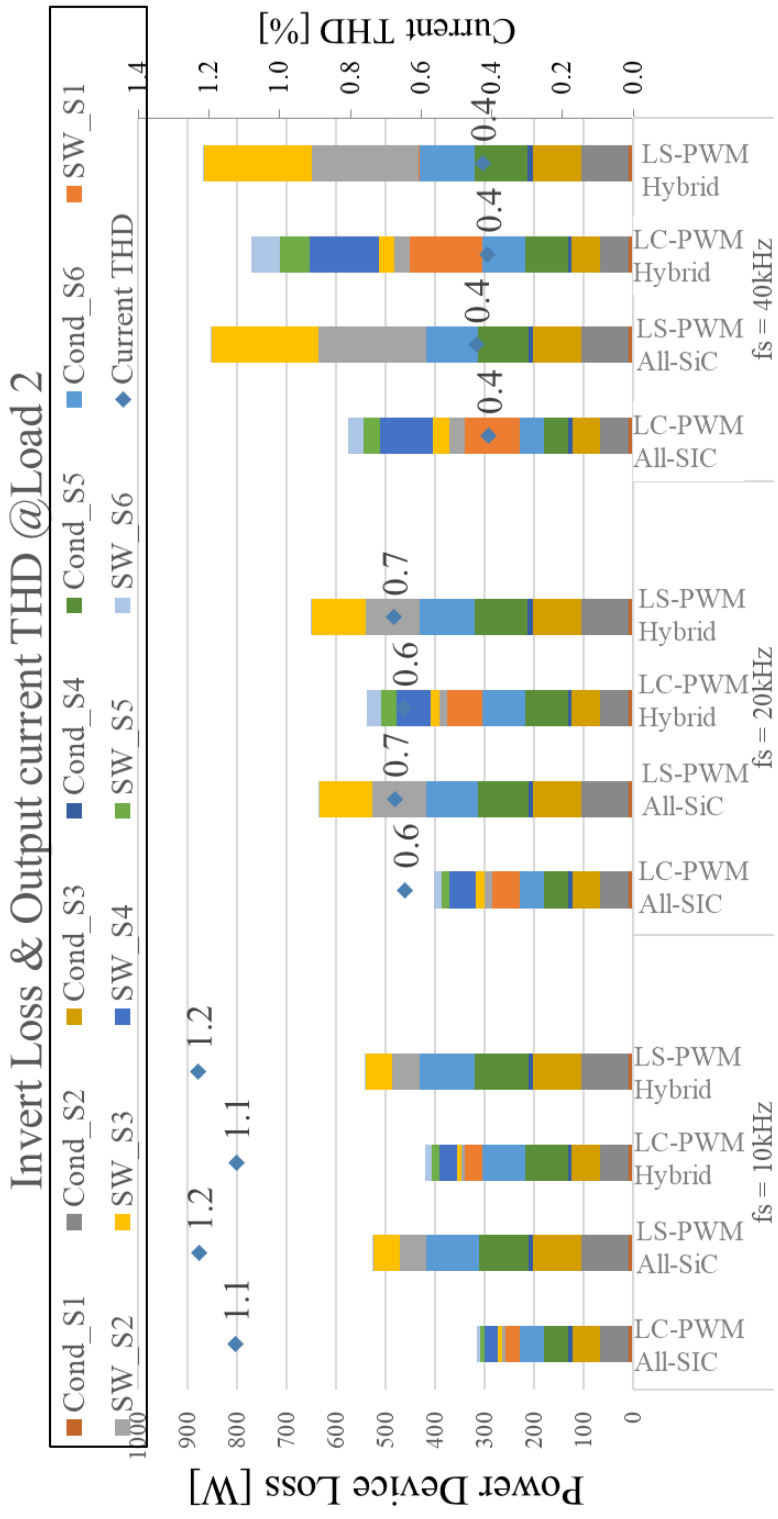


Figure 5.65 (a) V-I characteristics (b) switching loss of Si-IGBT/diode and SiC-MOSFET for 3L-ANPC

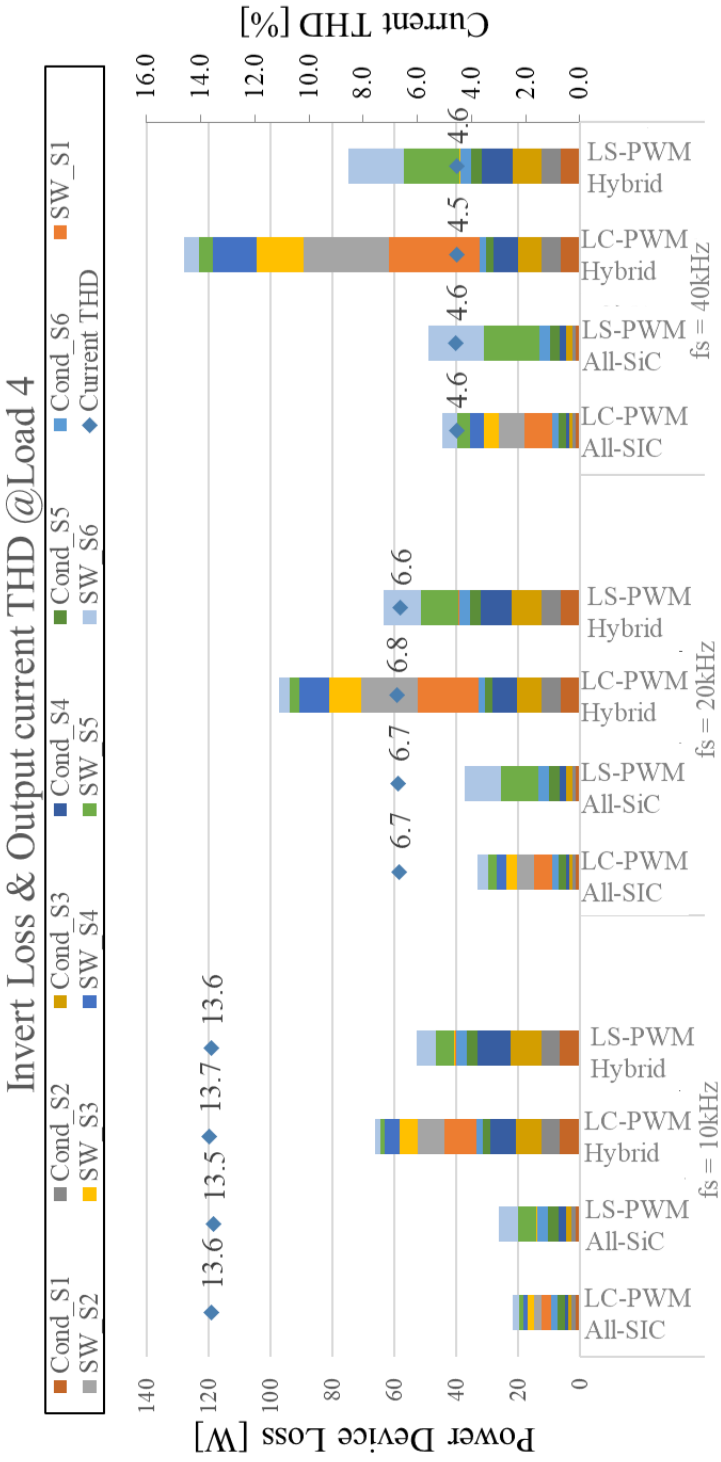
Considering the two topologies of the 3L-ANPC and their corresponding PWM strategies, we can ascertain the impact of inverter improvements. In the main points shown in Table 5.2, Point 2 represents a relatively low-speed region with high torque, implying a high current point. In contrast, Point 4 signifies a high-speed region with relatively low current. Figure 5.4 provides data comparing switching and conduction loss based on the inverter's PWM strategy at these two representative points out of the nine listed. The speed, torque, power, current, and voltage data for each load point is shown in Table 5.4.

Table 5.15. Two main load point condition.

Load	Speed [rpm]	Torque [Nm]	Power [kW]	Current [Apeak]	Voltage [Vpeak]
2	1,342.4	48.3	6.8	235.0	55.4
4	11,215.9	-11.9	-14.0	57.9	291.2


Invert Loss & Output current THD @Load 2
Cond_S1
Cond_S2
Cond_S3
Cond_S4
Cond_S5
Cond_S6
SW_S1
SW_S2
SW_S3
SW_S4
SW_S5
SW_S6
Current THD
Power Device Loss [W]
Current THD [%]
LS-PWM Hybrid
LC-PWM Hybrid
LS-PWM All-SiC
LC-PWM All-SIC
fs = 40kHz
fs = 20kHz
fs = 10kHz

(a)



(b)

Figure 5.66 Inverter loss simulation results depending on topologies, PWM strategies, and switching frequencies (a) at Load 2 (b) at Load 4.

As can be seen from the current and voltage values in Table 5.4, load point 2 is a low-speed, high-torque region, which is a high-current, low-voltage condition on the inverter side, i.e., the inverter MI is a small value. In addition, load point 4 is a high-speed, relatively low-torque region with low current and a large MI. From the results in Figure 5.4, several important points can be made.

1) THD is not greatly influenced by PWM strategies and topologies.: significantly impacted by switching frequency.
2) At low-speed, high-torque condition which means high current and low MI, conduction loss is dominant. At this point, LC-PWM has better efficiency with low conduction loss. (See Figure 5.4 (a))
3) At high-speed, low-torque condition which means low current and high MI, switching loss is dominant. At this point, LS-PWM has better efficiency for hybrid topology with low switching loss. (See Figure 5.4 (b))

Therefore, the effectiveness of the PWM strategy hinges significantly on the topology, which encompasses the characteristics of the power device and the conditions at the load point.

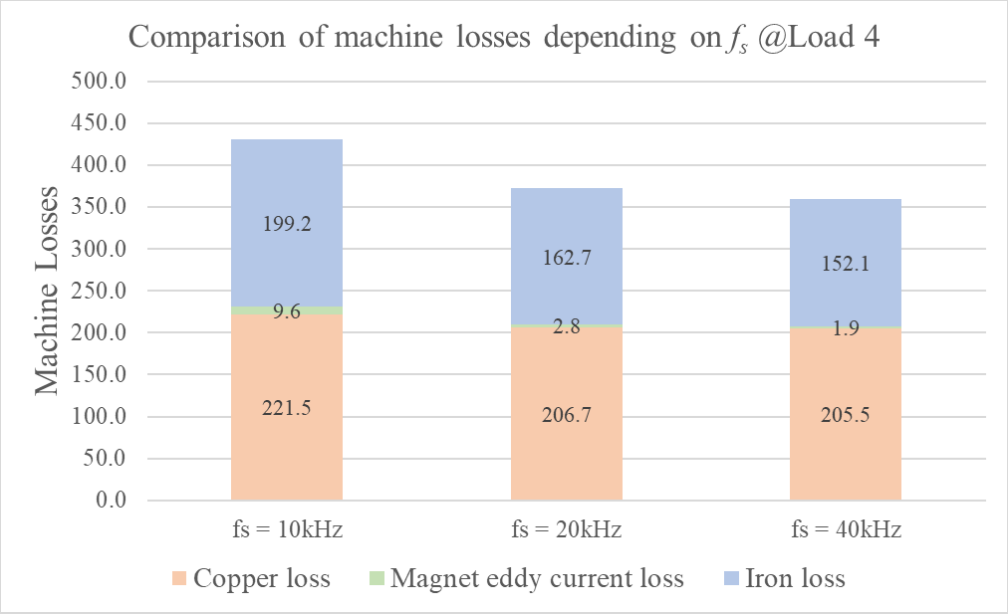
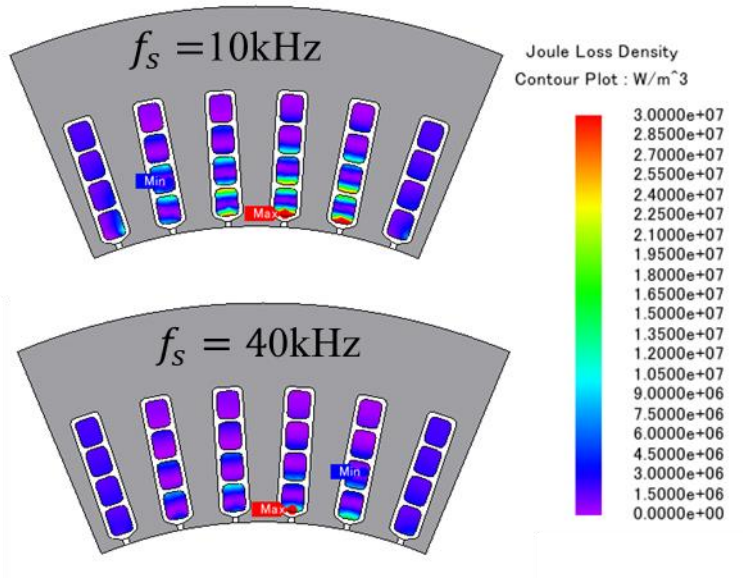
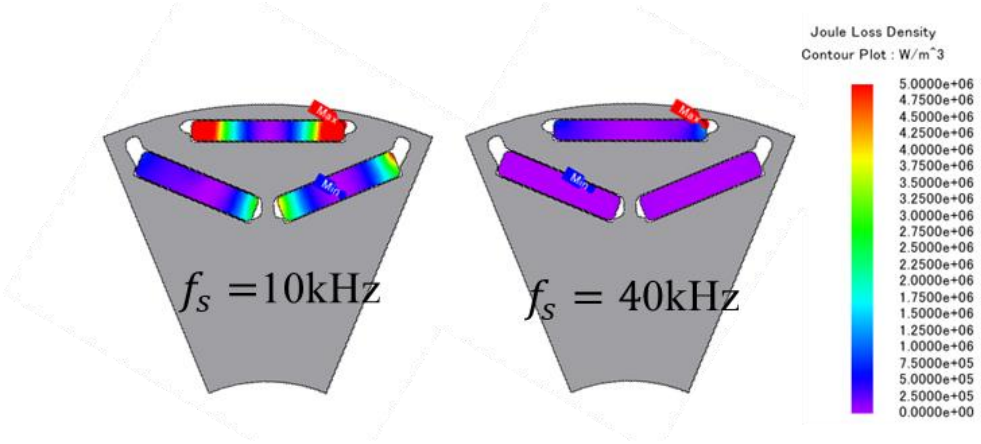


Figure 5.67 Machine loss simulation based on benchmark design (8pole) depending on switching frequency.



(a)



(b)

Figure 5.68 Comparison of loss simulation using JMAG-designer (a) AC Joule loss (b) Magnet eddy loss depending on switching frequency.

Figure 5.5 displays the results of analyzing the existing machine model with the extracted current data at load 4 which is high speed region. Additionally, a comparison of AC joule loss in stator coil and magnet eddy current loss are presented in Figure 5.6. As depicted in Figure 5.4 (b), it becomes evident that the THD of the output current experiences an improvement as the switching frequency escalates. This increment in the switching frequency paves the way for a consequential reduction in motor losses. In figure 5.4 and 5.5, the impact of THD on machine losses is quite substantial, as demonstrated by

a THD current of about 13.5% causing a significant difference in machine loss. A comparative study is depicted in Figure 5.6, wherein the results of current input at a frequency of 10 kHz are contrasted with the current input at a frequency of 40 kHz. As the frequency increases, enhancements can be observed in the magnet eddy current loss distribution and AC loss distribution of the coil. Thus, optimizing the PWM strategy in conjunction with switching frequency adjustments can substantially enhance the energy efficiency and performance of the electric drive system.

Considering the two topologies of the 3L-ANPC and their corresponding PWM strategies, we can ascertain the impact of inverter improvements. In the main points shown in Table 5.2, Point 2 represents a relatively low-speed region with high torque, implying a high current point. In contrast, Point 4 signifies a high-speed region with relatively low current. Figure 5.4 provides data comparing switching and conduction loss based on the inverter's PWM strategy at these two representative points out of the nine listed.

The methodology presented in Chapter 4 indicates that the maximum designable pole number is subject to change with the increase in switching frequency. In the current design, as the number of poles increases, a Table 5.4 presents the combinational possibilities of equivalent series turns per phase that can be designed in the hair-pin type. Design improvements are implemented by augmenting the n_p from the current 48 slots of 8 poles. Feasible alternatives are models with 10-pole and 12-pole configurations, and beyond these, performance may decline due to magnetic saturation within a confined size. Given that the theoretical optimal number of turns n_T computed from Equation 4.7 approximates to 40, the design was implemented with a combination of 40 turns for 10 poles over 60 slots. This approach aids in optimizing the design by aligning with the limitations of the system while ensuring improved performance and efficiency.

Table 5.16. Improved design for n_p and n_T for machine.

Pole	Slot	Layer per slot	Parallel circuit	Turns per phase
8	48	4	1	32
	48	6	1	48
	48	8	2	32
10	60	4	1	40
	60	6	2	30

	60	8	2	40
12	72	4	1	48
	72	6	2	36
	72	8	2	48

After selecting the suitable number of poles and slots, the first design parameter to consider due to the increase in the number of poles is the rotor's outer diameter D_r. Since the stator's yoke width that can be designed has decreased due to the increased number of poles, an effort to reduce copper loss is undertaken by increasing D_r. The performance results are contrasted by enlarging the D_r from the original design parameter of 84mm, specifically focusing on the peak torque value at the maximum torque point and the total motor loss at load points 2 and 4. This relationship is depicted in Figure 5.7. From this analysis, it can be observed that the peak torque reaches its maximum when D_r is 89mm, and the loss in the load is minimized around the 90mm.

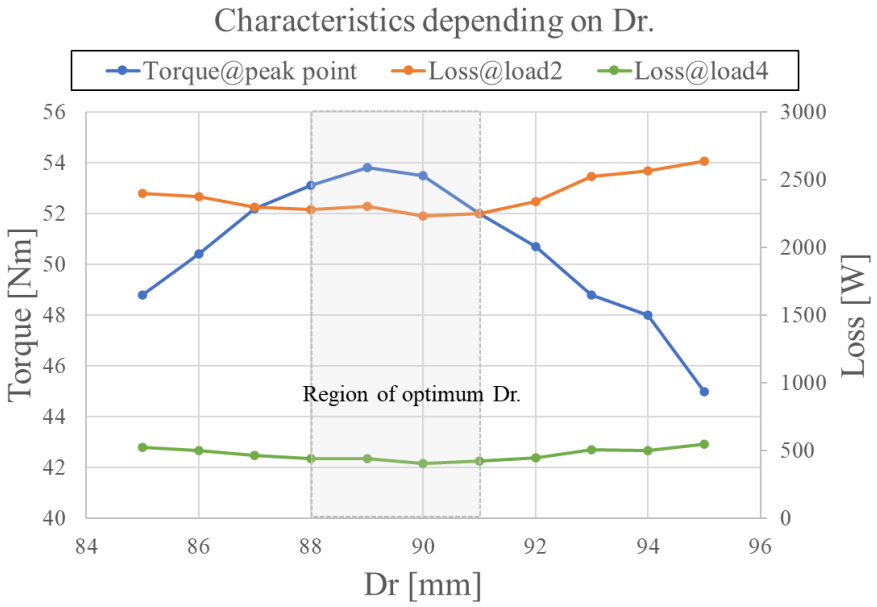


Figure 5.69 Peak torque, total loss at load 2, and total loss at load 4 depending on rotor diameter.

Based on these results, D_r is set and for other geometric design proposals, JMAG designer optimization is employed for the design process. A comparison of the final design and the original design is depicted in Figure 5.8. The main dimensions are verified in Figure 5.8.

5.1.3 Energy Loss Improvement Results

As the number of poles increased, the yoke width was diminished from 8.40mm to 7.10mm, and the outer diameter of the rotor was expanded to 89mm, as illustrated in Figure 5.7. Compared to the benchmark design, the total magnet usage was reduced by 2.5%, resulting in improved outcomes. By elevating the number of equivalent series turns from 32 turns to 40 turns, the overall flux linkage was enhanced, and accordingly, the maximum current value was reduced from 180 Arms to 158 Arms. This led to a decrease in the coil's cross-sectional area while maintaining the same current density.

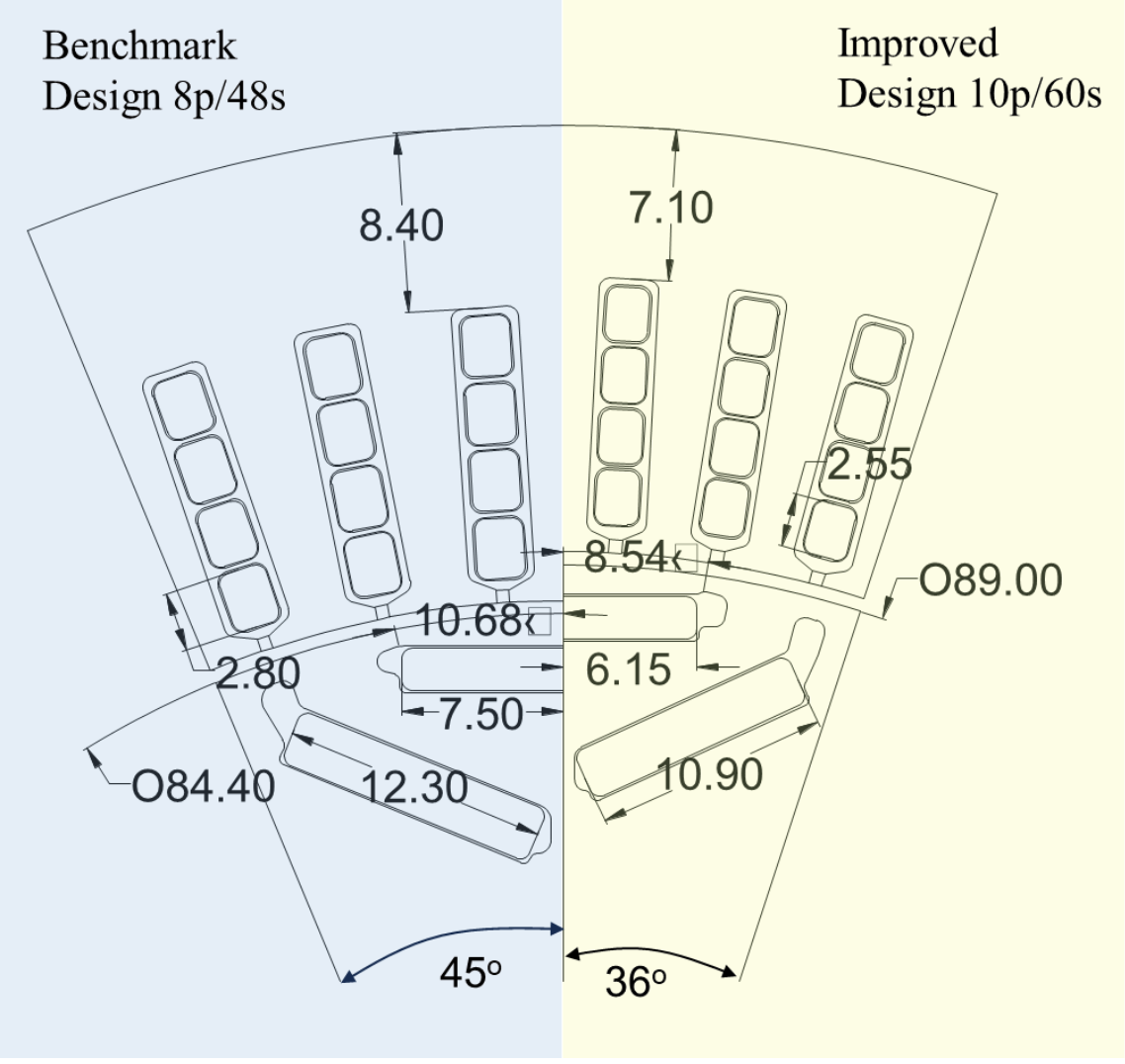


Figure 5.70 Comparison of main geometry for the machine design between benchmark and improved.

Table 5.17. Comparison of inverter and machine loss at each load point.

No.	Time [sec.]	Speed [rpm]	Toq. [Nm]	Inverter loss [W]			Machine loss [W]		
				Benchmark	All-SiC	Hybrid	Benchmark	All-SiC	Hybrid
1	1.2	1640.9	21.2	211.5	219.6	376.2	522.1	510.1	511.7
2	2.7	1342.4	48.3	888.6	975.0	1504.9	2561.7	2380.1	2374.3
3	8.6	5815.1	-44.5	671.6	836.7	1229.8	2186.2	2090.7	2090.4
4	12.9	11215.9	-11.9	85.6	123.5	193.6	582.2	402.8	404.6
5	22.4	2094.8	-8.6	57.1	71.1	129.3	102.1	99.4	99.9
6	36.6	9186.7	-3.3	20.4	23.4	42.0	222.8	112.1	112.8
7	42	7789.6	-5.9	38.4	48.5	84.4	286.9	134.8	134.3
8	77.9	6490.6	-6.0	38.9	48.9	86.0	215.1	114.8	114.5
9	195	5105.2	-4.5	27.4	32.7	59.4	102.6	68.7	68.0

Table 5.18. Comparison of energy loss during driving cycle US06.

No.	Time [sec.]	Speed [rpm]	Torque [Nm]	Energy loss [kJ]		
				Benchmark	All-SiC	Hybrid
1	1.2	1640.9	21.2	0.9	0.9	1.1
2	2.7	1342.4	48.3	9.3	9.1	10.5
3	8.6	5815.1	-44.5	24.6	25.2	28.6
4	12.9	11215.9	-11.9	8.6	6.8	7.7
5	22.4	2094.8	-8.6	3.6	3.8	5.1
6	36.6	9186.7	-3.3	8.9	5.0	5.7
7	42	7789.6	-5.9	13.7	7.7	9.2
8	77.9	6490.6	-6.0	19.8	12.7	15.6
9	195	5105.2	-4.5	25.4	19.8	24.8
Total energy loss during driving cycle [kJ]				114.7	90.9 (20.7% ↓)	108.3 (5.6% ↓)

The final geometry prompts a linked analysis of the inverter and machine using the JMAG-RT model. For this analysis, a frequency of 32 kHz is selected, given that it corresponds to the minimum system energy loss as identified using JMAG-RT. The outcomes of this analysis for two inverter topologies at each load point are compared with results derived from the original design, as documented in Table 5.6. Upon increasing the switching frequency from 12 kHz to 32 kHz, there's a slight increase observed in inverter losses. Nevertheless, the overall energy losses across the entire driving cycle are reduced

due to the improvements made in the machine design. In the All-SiC topology, implementing a combination with LC-PWM yielded a substantial loss reduction of 20.7%. Similarly, the hybrid topology facilitated a decrease in total energy loss by 5.6%. These findings underscore the positive influence of switching frequency and inverter topology selection on the system's overall energy efficiency, further highlighting the advantages of strategic design modifications.

5.2 Case Study B: 800V BEV Traction System

Active research is being conducted into high-volage BEV technologies, such as the 800V systems seen in vehicles like the Porsche Taycan or recent Hyndai Ioniq models [108,109], with the aim to enhance both the vehicle's range and the speed of battery charging [110]. As outlined in [110], the 800V system allows the machine to operate at higher voltage limits compared to the conventional 400V system, enabling high-speed operation and reducing losses due to decreased copper loss in the machine wire resulting from lower current. However, certain design modifications are required to accommodate this higher voltage. Specifically, the power components of the inverter must be designed to withstand an 800V load, which necessitates the use of a device with a safety margin rated voltage of 1200V. In addition, designs must also account for strengthening insulation, such as using high-voltage materials like polyimide for motor wire coating, and increasing the thickness of this coating [111]. The implementation of WBG devices in inverters can be more effective for enhancing efficiency at 800V. Furthermore, the problem of needing to use a power device with a high voltage rating can be addressed by using a multi-level inverter topology such as 3L-ANPC. This case study showcases the enhancements achieved through an integrated inverter-machine design that takes into account the interaction aspects of traction drive in an 800V BEV system. The study makes use of SiC devices and 3-level ANPC topologies to pinpoint optimal switching frequencies and PWM strategies, and presents improved machine designs tailored for these increased switching frequencies. The focus is on energy-efficient optimization design with a particular emphasis on driving cycles WLTC Class 3. This is accomplished through the DOE method.

5.2.1 Benchmark Design

The benchmark specification of the 800V traction model is provided in Table 5.8. The design of the inverter in this case-study utilizes a traditional 2-level half-bridge topology. The power device in this configuration is made up of Si-IGBTs. The thermal limitations associated with IGBTs necessitate the setting of the switching frequency at 12kHz. The machine design in this context involves an IPMSM. Notably, this design features a hair-pin type winding. This specific winding configuration is beneficial as it allows for enhanced power density. This enhancement is largely due to a higher fill factor within the slot compared to the traditional circular distributed windings.

Table 5.19. Benchmark specification of 800V traction model

Item		**Specification**
Peak power / torque		120kW / 195Nm
Nominal DC-link voltage		640Vdc
Maximum speed		16,500rpm
Inverter	Topology	2 level-half bridge
	Power device	Si-IGBT / diode
	Switching frequency	12kHz
Machine	Pole / slots	8 / 48
	No. of series turns per phase	32 turns
	Winding type	Hair-pin rectangular wire

The profile of drive cycle for machine points are calculated based on the WLTP3 cycle as depicted in Figure 3.4(a). This calculation employs vehicle dynamics as defined in Equations 3.1 to 3.7, along with the data provided in Table 3.2. The key points identified through the energy gravity center method are subsequently visualized in Figure 3.6. By utilizing the energy gravity center method, it becomes possible to identify key points of energy usage and distribution throughout the WLTP3 cycle.

5.2.2 Improve Design Using DOE Method

Figure 5.9 illustrates an energy optimization process utilizing the DOE method. The evaluation criterion, which is the load point of the driving cycle, is calculated first. Following this, the 3L-ANPC inverter, two PWM strategies, and topologies are employed to design the inverter and motor's poles and turns, based on the switching frequency. This

result, however, does not yet represent an optimized state; instead, it simply indicates a rough direction for design. Subsequently, the DOE method is applied to optimize the machine's detailed geometry, the inverter's switching frequency, and the PWM strategy. DOE provides a valuable framework for handling the complexity and the interdependencies of different machine parameters. DoE is a statistical method used to plan, conduct, analyze, and interpret controlled tests. It enables the efficient exploration of the design space by evaluating the influence of multiple variables and their interactions on the performance of a system [112]. For this reason, many studies have used DOE methods in machine design optimization [113,114].

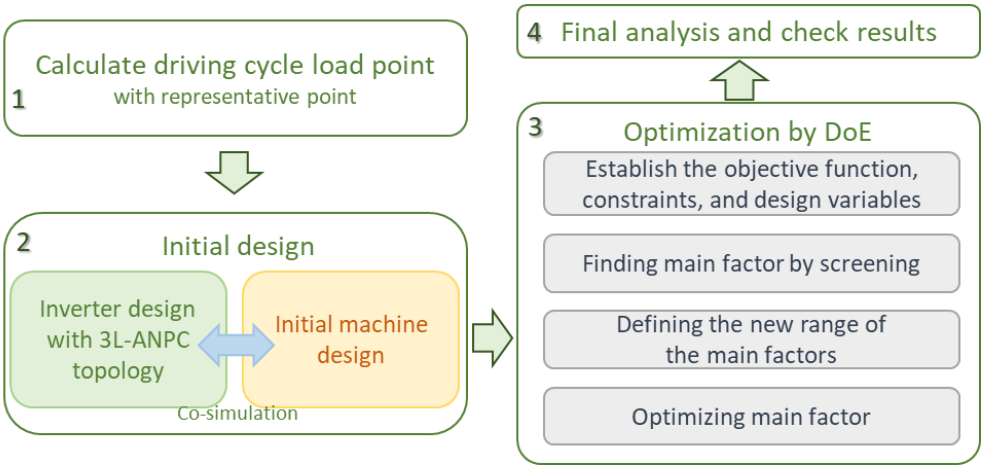


Figure 5.71 Design process for energy efficient 800V electric drive with DOE.

The DoE process starts by identifying the key design variables or factors, and the levels at which they will be varied. Next, an experimental design is constructed to define which combination of factor levels to test. These tests are then executed, and the data is analyzed to understand the effect of each factor and their interactions on the motor performance. In this study, based on this process, the interdependence of inverter and machine parameters using a simple DOE method analyzed and proceeded with the optimal design considering them.

The initial improvement design proceeds in the same manner as described in previous chapters. In the case of an 800V system, as studied in chapter 2, the advantages of WBG semiconductors and multi-level topology can be fully leveraged in the inverter design. Interestingly, even with an 800V system, it's feasible to use 600-650V power devices, the same grade used for a 400V system, by employing a 3L-ANPC inverter.

The peak torque and continuity of output power are verified by adjusting the number of poles and turns at an increased switching frequency of 800V. Figure 5.10 schematically displays the speed-torque curve capability according to designs of 8 pole 48 slots, 10 pole 60 slots, and 12 pole 72 slots. With the 10/60 pole-slot combination, the maximum output at high speed is slightly reduced, but there is less copper loss due to an increase in maximum torque capability. On the other hand, the design with 12 poles and 72 slots shows a noticeable reduction in maximum output power. Therefore, the 10-pole model is chosen as the initial design for improvement, and the optimization process is initiated accordingly.

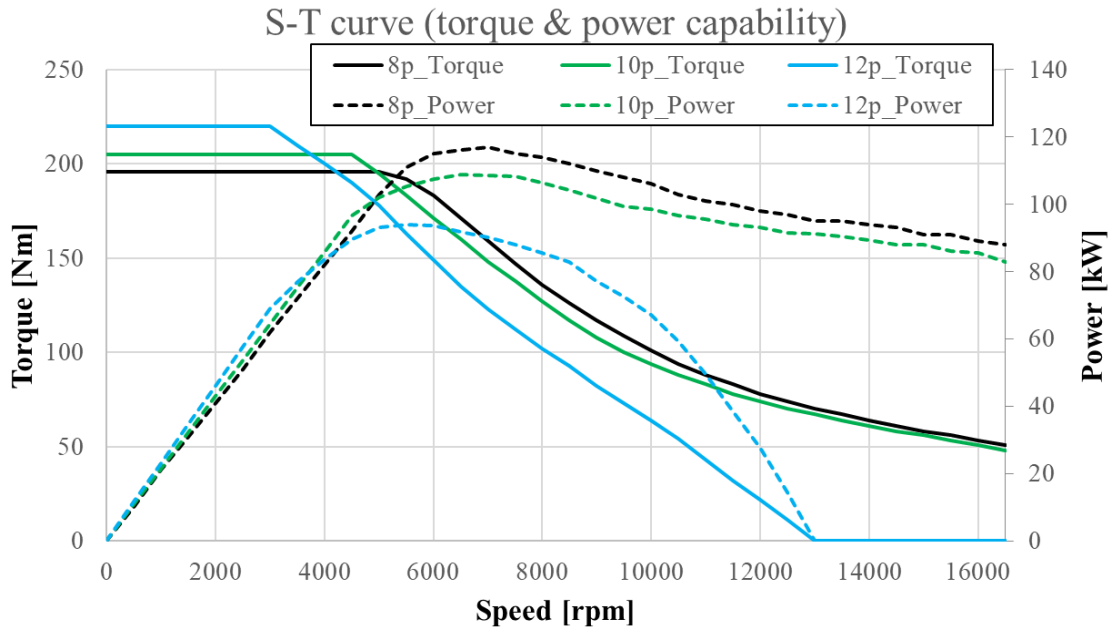


Figure 5.72 Speed-torque characteristics of the different pole and slot number with 8/48, 10/60, and 12/72.

The first step of the optimization utilizing DOE is to establish the objective function. The main objective function for optimization is minimizing 2 out of 10 representative points shown in Equation 5.1 exert the most significant influence on the overall drive cycle loss:

1. Load 1: 2185.2rpm, 99.7Nm for 106sec. duration; low-speed, high-current
2. Load 2: 8537.4rpm, 22.9Nm for 136sec. duration; high-speed, low-current

$$minimize\ F_{obj} = \sum Loss_{load1} + \sum Loss_{load3}$$ Equation 5.42

The next step is the specification of design parameters. These are the variables or factors that can be manipulated during the design process to influence the system's performance. In order to optimize the system, there are six geometric design variables of the machine and two variables for the inverter that need to be considered. The initial configuration and design variables for the machine are depicted in Figure 5.11 and are initialized with low and high values as specified in Table 5.9. It is important to ensure that the design constraints do not exceed the limitations of the existing magnet usage and copper utilization while also taking into account manufacturing constraints such as fill factor and cost considerations. Additionally, it is crucial to maintain an acceptable current density of the wire in consideration of the thermal characteristics.

- Fixed pole/slot combination for noise and vibration characteristics.
- Fixed current density: coil width is dependent on the coil height.
- Fixed slot fill factor (<58%) (defined by total bare copper area per slot area).
- Less weight of magnet and copper than benchmark design (in Table 1).

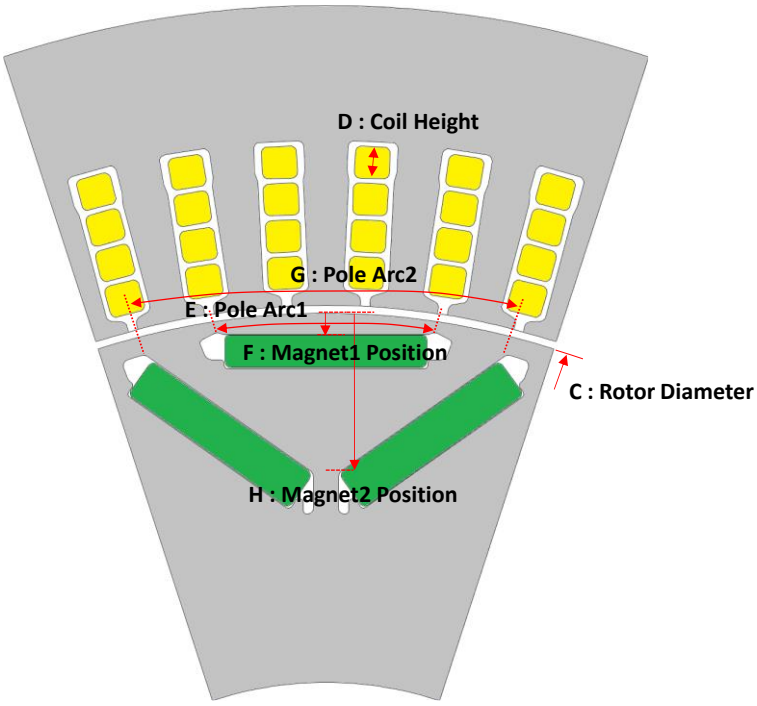


Figure 5.73 Initial improved design of machine and design variable for machine geometry.

Table 5.20. Design variables, initial value and 2-level variation range

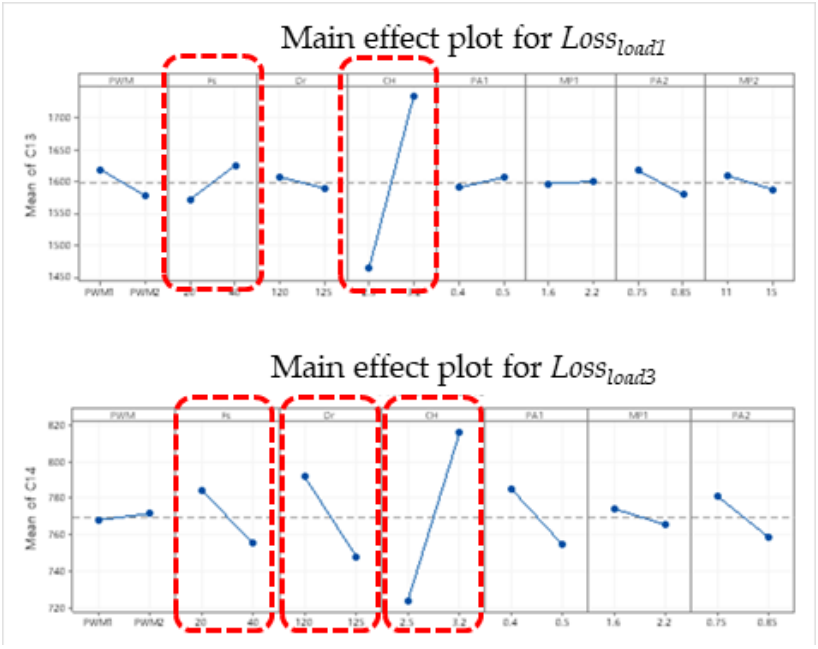
Variable	Definition	Initial	Level low	Level high
A	PWM strategy	-	LC-PWM	LS-PWM
B	Switching frequency (kHz)	30	20	40
C	Rotor diameter (mm)	122.5	120	125
D	Coil height (mm)	2.85	2.5	3.2
E	Pole arc1 ratio	0.47	0.4	0.5
F	Magnet 1 position	1.7	1.5	2.2
G	Pole arc2 ratio	0.82	0.75	0.85
H	Magnet 2 position	13	11	15

In this study, a fractional factorial design with two levels and eight factors is utilized to minimize the number of experiments for finding the main design factors impact on the energy loss as screening method [112]. The objective function includes the total loss, which encompasses switching and conduction losses in the inverter, as well as copper, iron, and magnet eddy losses in the machine. Using a 1/16 fractional factorial design allows conducting experiments based on a $2^{(8-4)}$ scheme, thus reducing the number of required experiments significantly.

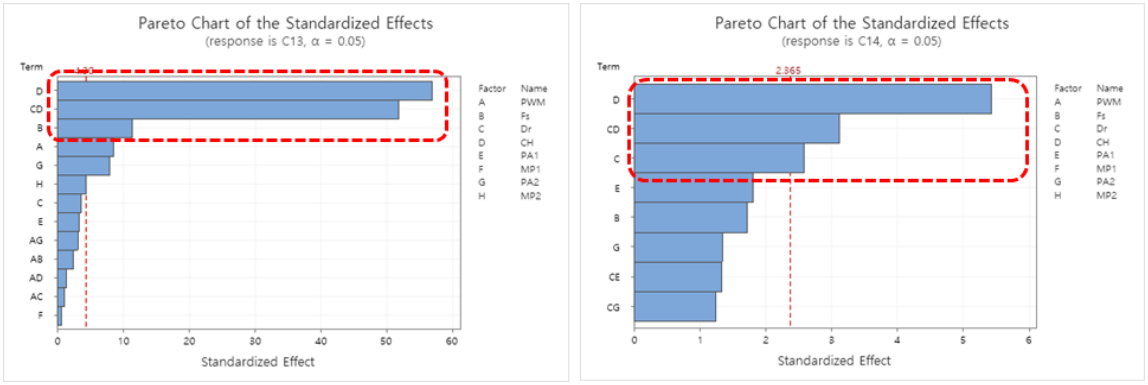
Table 5.21. 1/16 fractional factorial design and resutls

No.	Factor level combination	Loss@load1	Loss@load2
1	A1-B1-C1-D1-E1-F1-G1-H1	1615.9	843.2
2	A2-B1-C1-D1-E1-F2-G2-H2	1490.2	747.5
3	A1-B2-C1-D1-E2-F1-G2-H2	1621.4	733.3
4	A2-B2-C1-D1-E2-F2-G1-H1	1648.7	764.4
5	A1-B1-C2-D1-E2-F2-G2-H1	1338.5	689.7
6	A2-B1-C2-D1-E2-F1-G1-H2	1304.0	719.5
7	A1-B2-C2-D1-E1-F2-G1-H2	1369.7	645.2
8	A2-B2-C2-D1-E1-F1-G2-H1	1313.6	651.2
9	A1-B1-C1-D2-E2-F2-G1-H2	1622.9	789.8
10	A2-B1-C1-D2-E2-F1-G2-H1	1558.4	772.5
11	A1-B2-C1-D2-E1-F2-G2-H1	1655.9	825.7
12	A2-B2-C1-D2-E1-F1-G1-H2	1635.7	855.2
13	A1-B1-C2-D2-E1-F1-G2-H2	1809.9	849.4
14	A2-B1-C2-D2-E1-F2-G1-H1	1825.8	862.7
15	A1-B2-C2-D2-E2-F1-G1-H1	1907.4	768.5
16	A2-B2-C2-D2-E2-F2-G2-H2	1842.7	798.7

The details of the fractional factorial design and the corresponding results are presented in Table 5. Figure 5.12 illustrates: (a) the effect of each factor on the loss at load1 and load 2, and (b) Pareto charts for the loss at load 1 and load 2. The Pareto chart, shown in (b), combines the non-effective factors for analysis. For both load points, the most influential factors are identified as B: switching frequency, C: rotor diameter and D: coil length.



(a)



(b)

Figure 5.74 (a) Main effect plot (b) Pareto chart for finding main factors influencing on loss at load 1 and load 2.

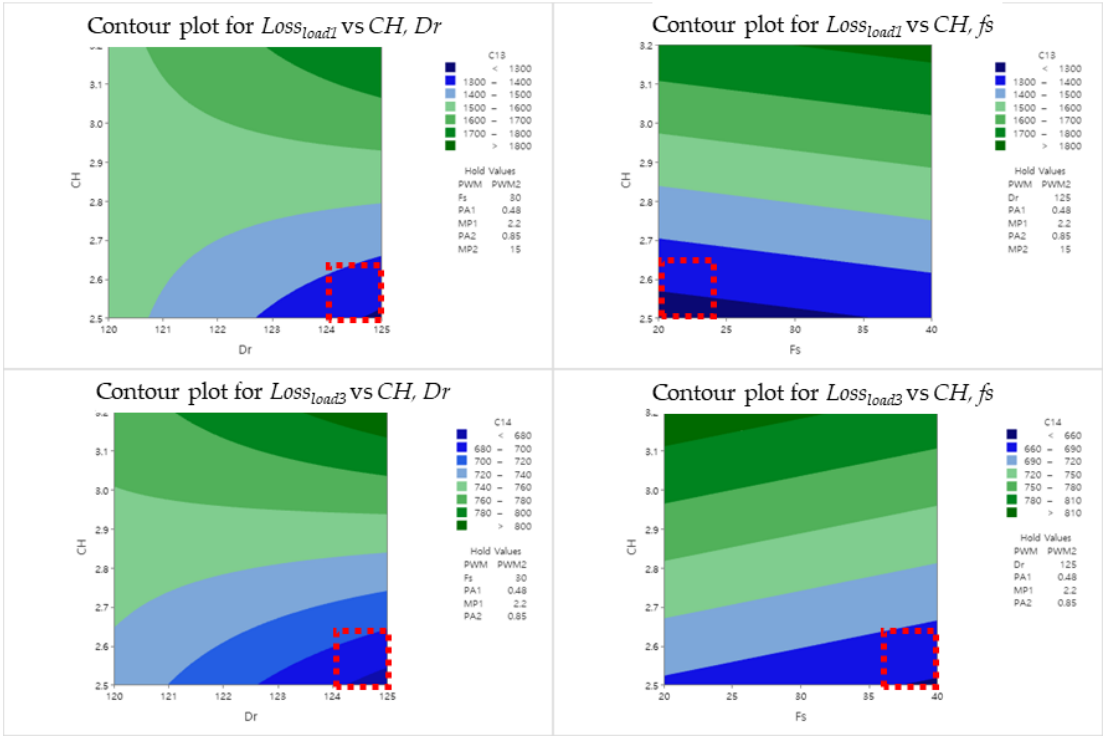


Figure 5.75 Contour plot for loss at load 1 and load 2 vs *CH*, D_r, and f_s; min. of *CH*, max. of D_r and another optimum point of f_s indicates minimizing objective function.

In the context of this research, the optimization process concentrates on the examination of three primary factors, derived from the results of the fractional factorial design, while maintaining other factors at a fixed level that facilitates loss minimization. Figure 5.12 delineates the optimization direction for factors B, C, and D. To enhance the range of the high level for factor C and the low level for factor D, the response surface method (RSM) is implemented. In this process, a central composite design (CCD) is employed, incorporating a total of 15 designs (2^3+1+3×2) [115]. The finalized values for the design parameters are delineated in Table 5.13.

Table 5.22. Final optimized design value

Variable	**Definition**	**Initial**
A	PWM strategy	LS-PWM
B	Switching frequency (kHz)	24
C	Rotor diameter (mm)	126.5
D	Coil height (mm)	2.47
E	Pole arc1 ratio	0.48
F	Magnet 1 position	2.2
G	Pole arc2 ratio	0.85

Variable	Definition	Initial
H	Magnet 2 position	15

5.2.3 Energy Loss Improvement Results

Using the optimized design, simulations are performed for 10 representative points. As can be seen in Table 5.12, by incorporating a hybrid topology 3L-ANPC with a combination of SiC-MOSFET and Si-IGBT, the total energy losses of inverter can be reduced by 13.5%. Additionally, for the machine design, an energy improvement of 6.4% is attainable. As a result, a notable 7.7% reduction in total energy loss during the driving cycle is observed.

Table 5.23. Comparison of energy loss consumption between original benchmark and improved design

No.	Time [sec.]	Speed [rpm]	Toq. [Nm]	Inverter loss [W]			Machine loss [W]		
				Benchmark			Improve		
				Inv.	Mach.	Total	Inv.	Mach.	Total
1	106	2185.2	99.7	41.5	134.8	176.2	31.2	127.5	158.7
2	127	6914.3	33.5	11.6	84.0	95.6	10.2	82.0	92.2
3	136	8537.4	22.9	8.5	80.0	88.5	8.5	81.2	89.7
4	138	4036.4	57.3	23.1	89.3	112.4	19.8	80.7	100.5
5	143	1857.4	52.2	21.2	59.3	80.5	20.4	51.4	71.8
6	149	2578.7	-58.2	24.8	76.8	101.6	21.5	69.7	91.2
7	193	5388.1	5.3	2.5	37.4	39.9	2.5	32.4	34.9
8	241	1620.8	-6.3	3.2	10.9	14.1	2.8	10.1	12.9
9	274	44.4	29.9	21.4	35.5	56.9	19.6	33.5	53.1
10	293	3828.0	3.0	1.9	30.7	32.6	1.6	29.5	31.1
Total energy loss during driving cycle [kJ]				159.6	638.6	798.2	138.1 (13.5%)	598.0 (6.4%)	736.1 **(7.7%)**

5.3 Hybrid PWM Strategy

Chapter 5.1 confirmed that LS-PWM and LC-PWM present varying advantages in energy efficiency, contingent on the load conditions of the drive. This chapter capitalizes on this insight to analyze system efficiency according to the PWM strategy across the entire driving region. Leveraging the enhanced model designed in 5.1, this analysis seeks to discern the boundary between the two PWM strategies. The aim is to articulate a strategy that operates dual PWM based on sections or load conditions, rather than adhering to a

single PWM strategy throughout the entire driving cycle. This examination also includes the outcomes of any advancements achieved through these two combinations.

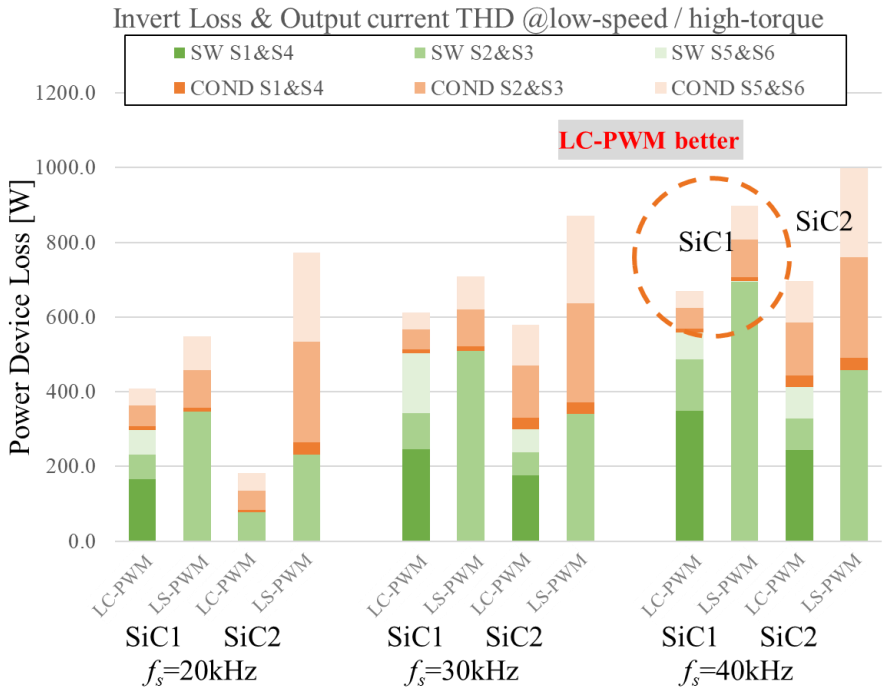
5.3.1 Loss Analysis Based on Load Condition

This study takes into account the All-SiC topology, and a thorough loss analysis for the two SiC-MOSFET devices, as detailed in Table 5.13, is once again carried out. Analogously, a co-simulation model is utilized, and comprehensive specifications for the two models are delineated in Table 5.13.

Table 5.24. Power device specification

Part No.	**SiC1 CM30015065D [92]**	**SiC 2 SCT3030AL [116]**
Manufacturer	Wolfspeed	Rohm
$V_{DS\,max}$ / $I_{D\,max}$	650V / 120A	650V / 70A
$R_{ds(on)}$	15mΩ	30mΩ
Eon (R_{ext}= 3.3Ω, I_D = 50A)	1,100µJ	730µJ
Eoff (R_{ext}= 3.3Ω, I_D = 50A)	500µJ	570 µJ

The same load point as in Chapter 4.1 is utilized, and an analysis of inverter and motor losses is executed for two areas: one characterized by high-speed and low-torque, and the other by low-speed and high-torque. This analysis aids in understanding how losses distribute across different operational conditions and forms the basis for optimizing the inverter and motor design according to specific load requirements.



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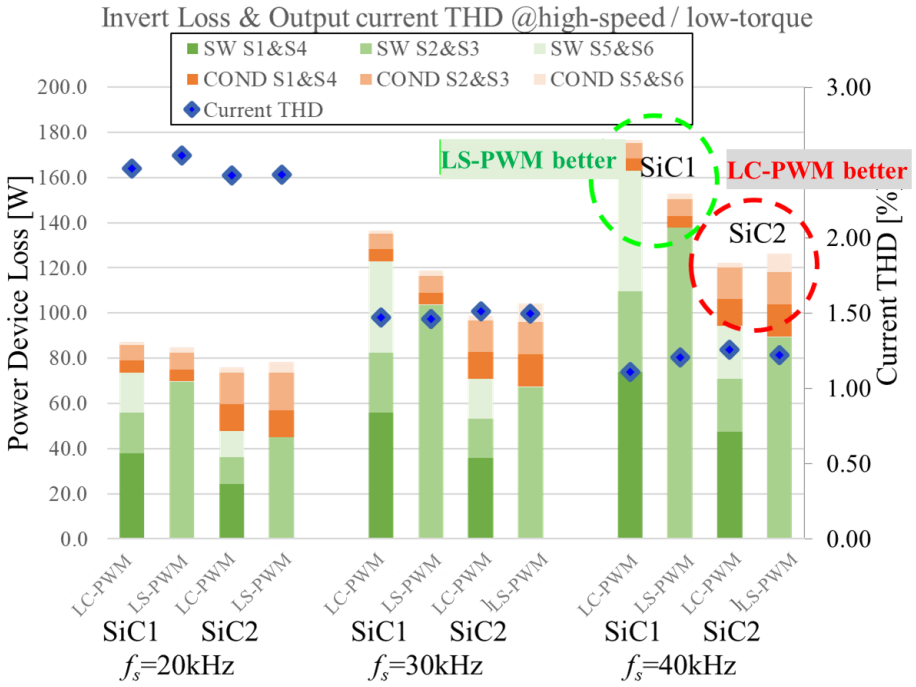


(b)

Figure 5.76 Inverter losses and output current THD results depending on PWM strategies and switching frequency in representative operating point (a) 1342rpm / 48.3Nm (b) 11,215rpm / 11.9Nm.

As depicted in Figure 5.14 (a), the region characterized by low speed and high torque, which equates to high current and low voltage output, favors the LC-PWM strategy. This strategy effectively curtails conduction losses in these conditions. On the contrary, in the region marked by high speed and low torque, as shown in Figure 5.14 (b), the LS-PWM strategy demonstrates superior performance when using the SiC1 device. However, when the SiC2 device, characterized by a significantly high on-state resistance, is employed, the prominence of conduction loss becomes more significant, thereby nullifying the advantage of the LS-PWM strategy. It's important to note that the THD of the output current is relatively independent of the choice of PWM strategy and is largely dictated by the switching frequency.

5.3.2 Comparison of Results

The simulation results for whole operating region delineate two distinct regions, depicted in Figure 5.15, wherein losses are optimally minimized by either LC-PWM or LS-PWM, specifically in the torque-speed plane. Thus, a comprehensive hybrid modulation approach for the entire machine operation region, grounded on control variables such as motor phase current and voltage. As demonstrated in Figure 5.15, the LS-PWM strategy is employed in region with comparatively smaller current, whereas the LC-PWM strategy is employed when the current is higher, and the conduction losses are significant. This hybrid PWM enhances the energy efficiency across the whole system and curtails cumulative losses inflicted on each power device. However, the outcomes, as represented in Figure 5.14, are contingent on the selection of power devices. Moreover, the load conditions of the motor, such as current phase angle, and voltage usage that is related to flux-weakening control, significantly influence the results.

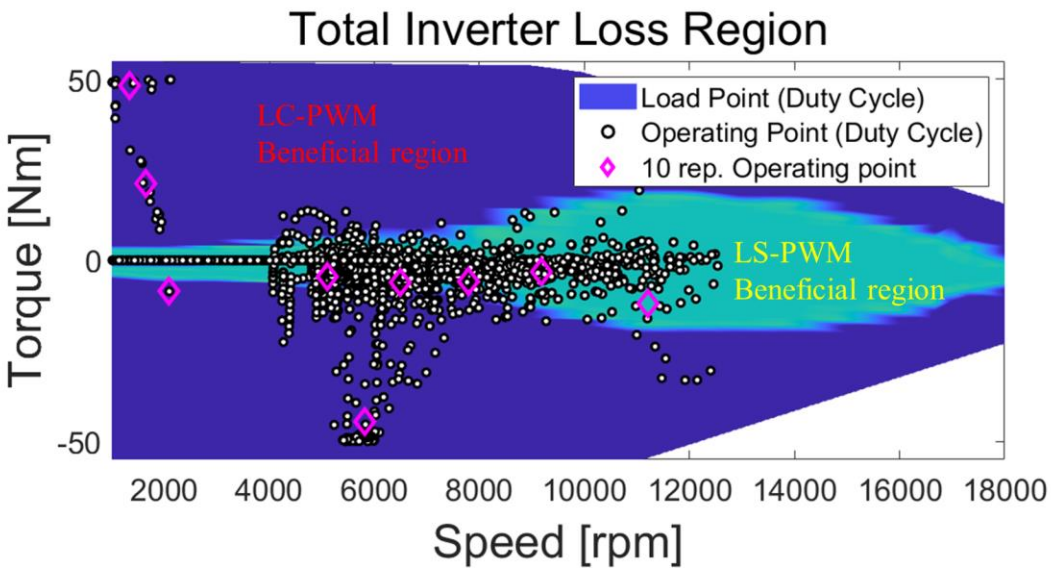
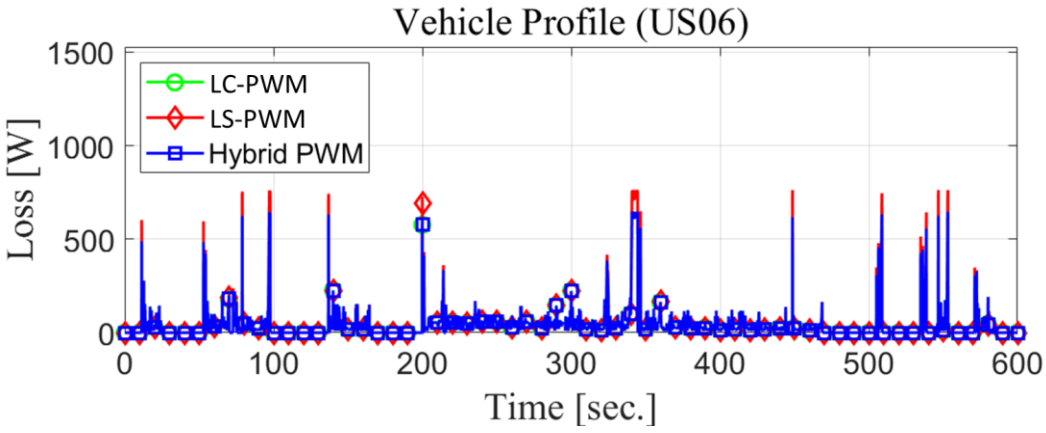
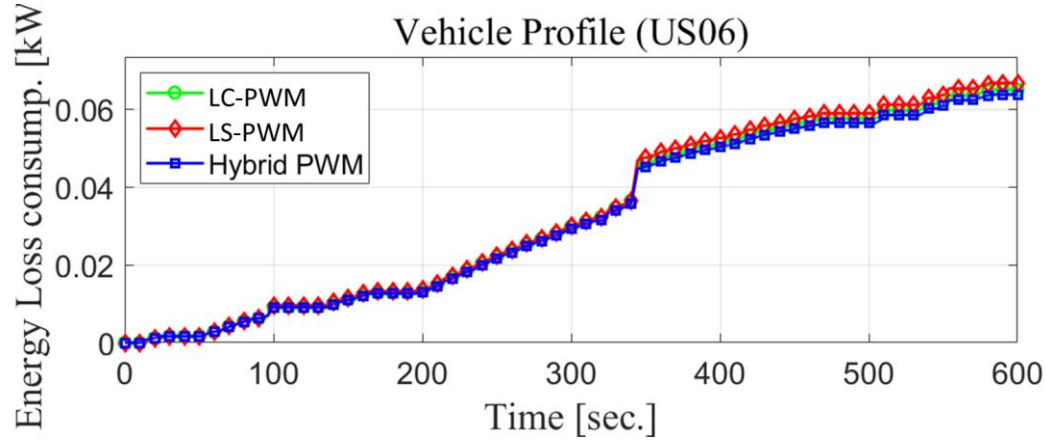


Figure 5.77 Indication of region where each strategy is advantageous in terms of losses across the entire drive range.

Figure 5.16 describes the accumulated energy loss consumption of ANPC inverter during the drive cycle, represented in units of kWh. As illustrated in Table 5.14, each drive cycle's energy loss consumption varies depending on the employed PWM strategy. In the case of the US06 cycle, a notable energy loss reduction of 3.2% can be observed when implementing the less loss-inducing of the two strategies. Moreover, the application of a hybrid modulation approach can lead to a substantial reduction in energy loss, measured at 0.0026kWh. Similar results are seen with the FTP_EPA75 Drive cycle, a combination of EPA UDDS and HWFET. Compared to using only LS-PWM, an energy savings of 0.0014kWh is achievable. When compared to using only LC-PWM, the savings are slightly less but still notable at 0.0009kWh. These reductions not only facilitate an increased driving range with a given battery system, but also enhance the inverter's operational reliability across the entire cycle.



(a)



(b)

Figure 5.78 (a) Inverter losses during US06 drive cycle in watt. (b) accumulated energy loss consumption in kWh depending on PWM strategy

Table 5.25. Energy consumption and improvement by using hybrid PWM on different drive cycle.

Cycle	Duration	Energy Loss (kJ)			Energy Loss (kWh)			Improve (%)
		LC-PWM	LS-PWM	Hybrid	LC-PWM	LS-PWM	Hybrid	
US06	600	39.0	39.3	37.7	0.0650	0.0655	0.0629	**3.2**
EPA_UDDS	1372	66.8	67.3	65.6	0.0487	0.0491	0.0478	**2.6**
HWFET	765	90.5	92.9	90.0	0.1183	0.1214	0.1176	**3.1**
FTP_EPA75	1874.3	98.1	99.0	96.3	0.0523	0.0528	0.0514	**2.7**
LA92	1435	90.5	91.0	88.8	0.0631	0.0634	0.0619	**2.4**

5.4 Summary

In this chapter, a pragmatic case study has been conducted leveraging the 3L-ANPC, WBG device, and motor design improvement methodologies presented in previous chapters. By applying an enhanced design to the high-speed B-ISG motor of the 400V PHEV system, it was possible to enhance energy efficiency by 20.7% using the All-SiC topology and by 5.6% when using the hybrid approach in the existing design. Verification of the final energy loss was accomplished utilizing a co-simulation model.

Additionally, the design enhancement process was carried out in a similar manner for the 800V BEV electric drive. In this context, the usage of DOE methodology was demonstrated to identify key parameters among inverter and motor variables, gauge their impact, and carry out optimal design. In the BEV design, it was confirmed that a 7.7% energy efficiency improvement could be achieved solely with the hybrid topology, while energy losses were mitigated in both the inverter and the motor.

Lastly, a hybrid strategy was proposed that leverages both LS-PWM and LC-PWM strategies in combination depending on the operating point. The advantages of this hybrid strategy across various driving cycles were elucidated. This approach capitalizes on the inherent strengths of both LS-PWM and LC-PWM, allowing for an adaptive response based on the specific requirements of the operating point, and thereby enhancing overall system efficiency.

6 Proof-of-concept Demonstration

In this chapter, the creation and examination of a single-phase 3L-ANPC topology, composed of SiC-MOSFETs, is straightforwardly described. The influence of PWM strategy and switching frequency was empirically validated through a Rapid Control Prototype (RCP). The PWM strategies examined in this research were effectively applied as gate signals to control an actual SiC-MOSFET device in real time through MATLAB SIMULINK, which served as the control platform for the RCP. To efficiently implement the two PWM strategies, the carrier-based SPWM method was employed.

The load conditions for the R-L load were varied to encompass scenarios such as high-speed-low-current and low-speed-high-current, corresponding to high MI and low current, and low MI with relatively higher current, respectively. These load points allowed for a comprehensive comparison of the two PWM strategies under different operating conditions.

Furthermore, an innovative hybrid SiC-GaN topology is devised, aiming to take advantage of the strengths of SiC and GaN while mitigating their respective weaknesses. A comparison was conducted between two parallel SiC configurations and the SiC-GaN hybrid topology, evaluating switching performance and efficiency to ascertain the benefits and potential drawbacks of these novel hybrid systems.

6.1 Experimental Setup

6.1.1 Hardware

Figure 6.1 presents the setup for the test hardware. A single-phase 3L-ANPC inverter, built with SiC- MOSFETs, is linked to a DC power supply, and the load setup consists of R-L loads using various series/parallel combinations. Real-time control can be implemented in Simulink using the Rapid Control Prototype model. By configuring the control logic and delivering the PWM signal to the gate driver, which is supplied with the external 24V DC power of the 3L-ANPC inverter, inverter operation can be facilitated. The input and output voltage and current can be measured using an oscilloscope and an external power analyzer.

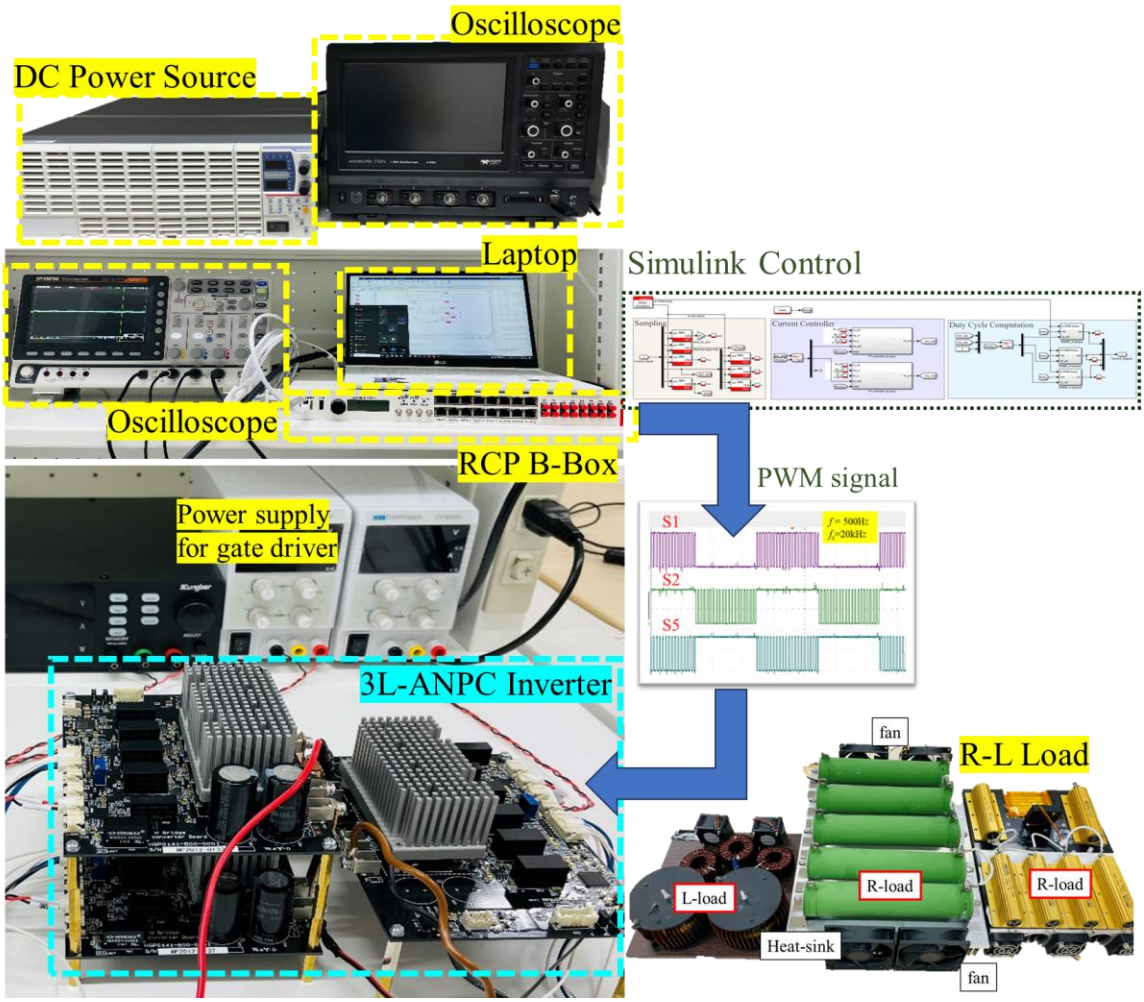


Figure 6.79 Experimental setup with RCP B-Box and 3L-ANPC

The specific 3L-ANPC topology used for testing is depicted in Figure 6.2. It's comprised of six switch sets of the SiC-MOSFET, with four electrolytic capacitors paralleled on both DC+ and DC-. The system includes a built-in gate driver, which operates on a 24V supply. The specifications associated with the 3L-ANPC inverter are presented in Table 6.1. The gate voltage for SiC-MOSFET switching, both for turning on and off, are +18V / -2V, and an external gate resistance of 3.3Ω is connected to each device. Each capacitor of C1 and C2, has a capacitance of approximately 500μF. In Figure 6.3, the configuration of the R-L load is illustrated, which is employed for implementing different load conditions.

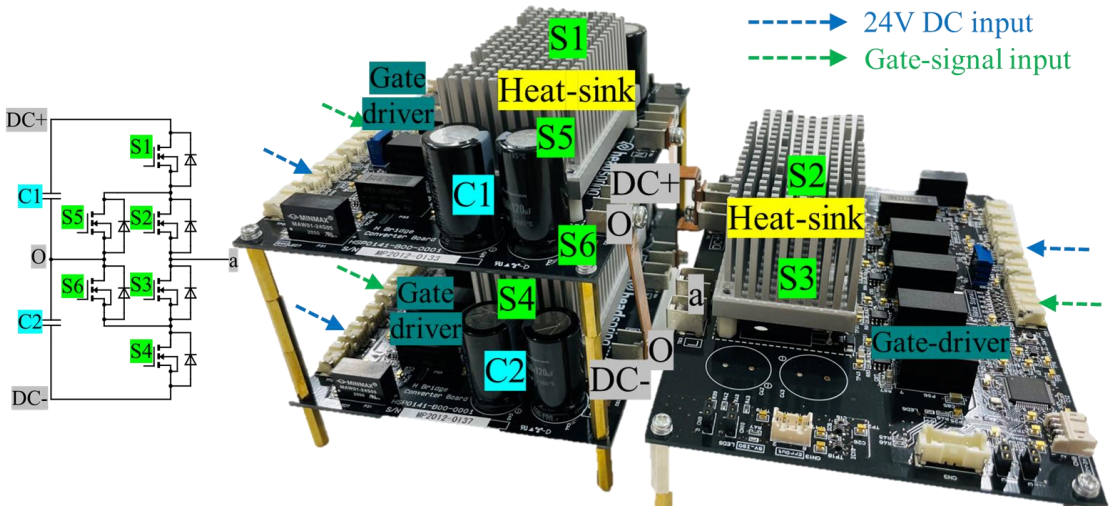


Figure 6.80 Single phase 3L-ANPC inverter

Table 6.26. 3L-ANPC Specification

Components	Specification	Remark
6-SiC-MOSFETs	SCT3030AL – Rohm	650V / 70A max.
Capacitor (C1, C2)	500µF each	450V 120µF – 4parallel +20µF film capacitors
External gate resistance	3.3Ω	-
Gate voltage	+18V / -2V	2.47

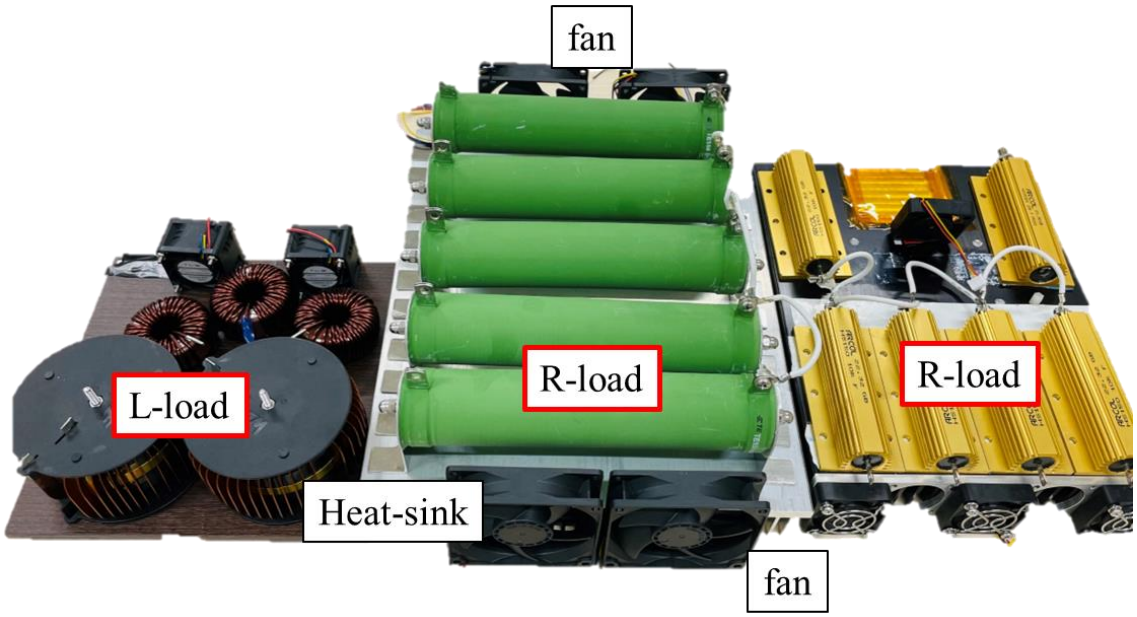
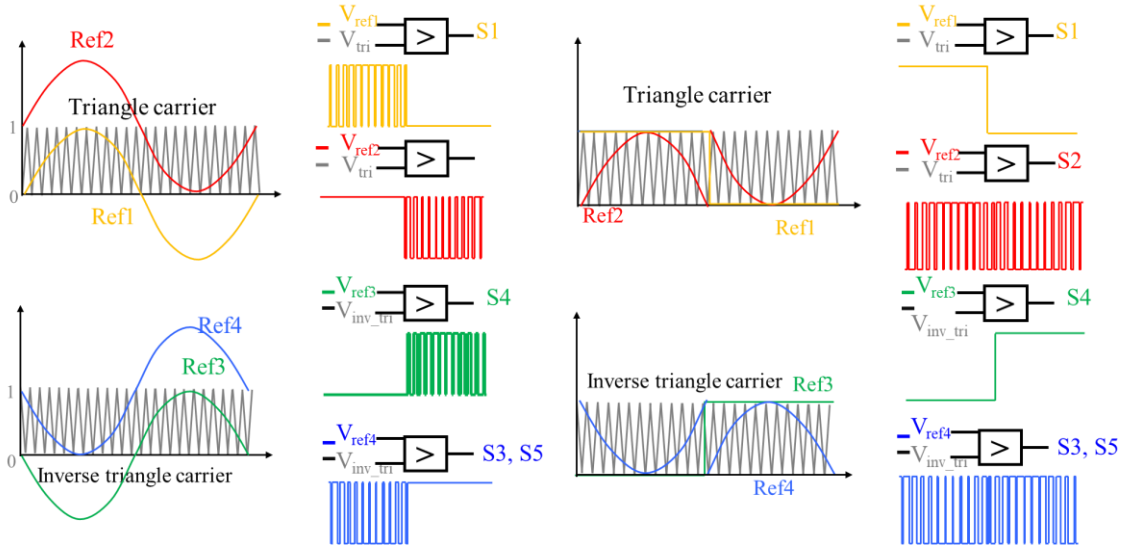


Figure 6.81 R-L load in parallel and series connection for different load conditions.

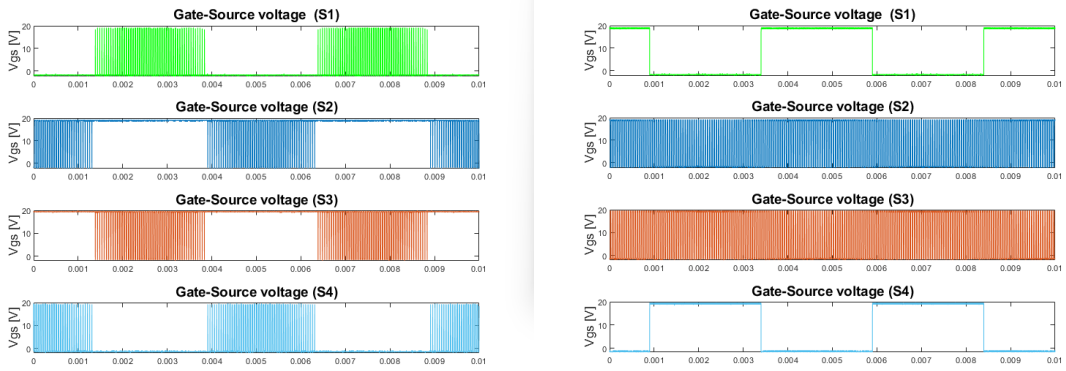
6.1.2 Modulation Signals

The Imperix RCP B-Box allows for real-time control by generating a gate signal. Two PWM strategies are implemented using the carrier-based SPWM method [117], as illustrated in Figure 6.4. Additionally, the implementation of PWM signal, as shown in Figure 6.5, is evaluated. A minimum feasible dead-time for operating without short circuit in the SiC-MOSFET is set to 600ns.



(a) (b)

Figure 6.82 PWM signal generating by SPWM (a) LC-PWM (b) LS-PWM



(a) (b)

Figure 6.83 Experimental PWM signal check generated by RCP B-Box (a) LC-PWM (b) LS-PWM

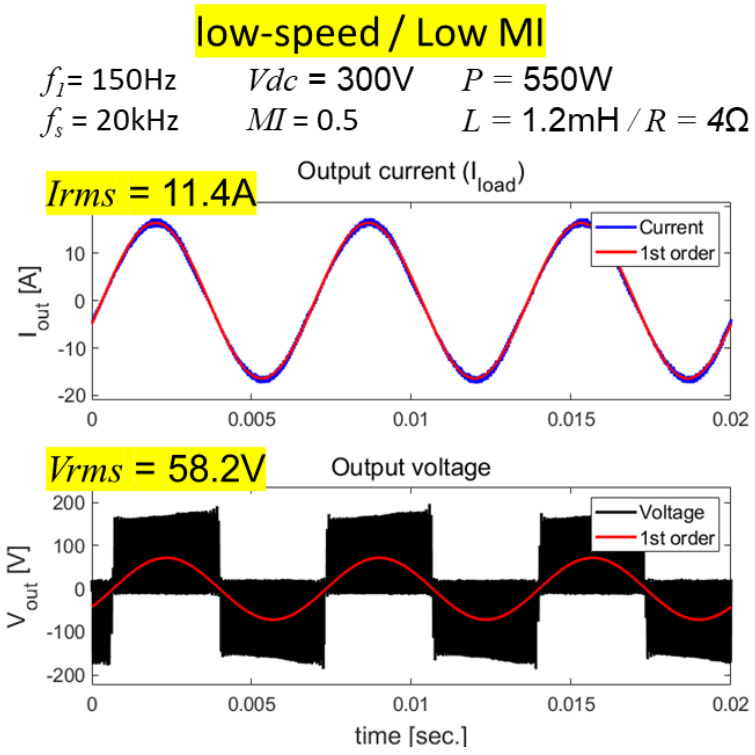
6.2 Experimental Results

The preceding simulation confirmed that the PWM strategy, which yields superior overall inverter efficiency, can be different based on load conditions. Particularly in conditions of relatively high current and low speed—that is, a low voltage level—conduction loss dominates, thus making LC-PWM more favorable. It was determined that sections heavily impacted by switching loss could see some advantage to LS-PWM. To verify this, two conditions were implemented using R-L load, and a fundamental frequency area was set where the two ranges could differ. The specific load conditions for comparison are shown in Table 6.2.

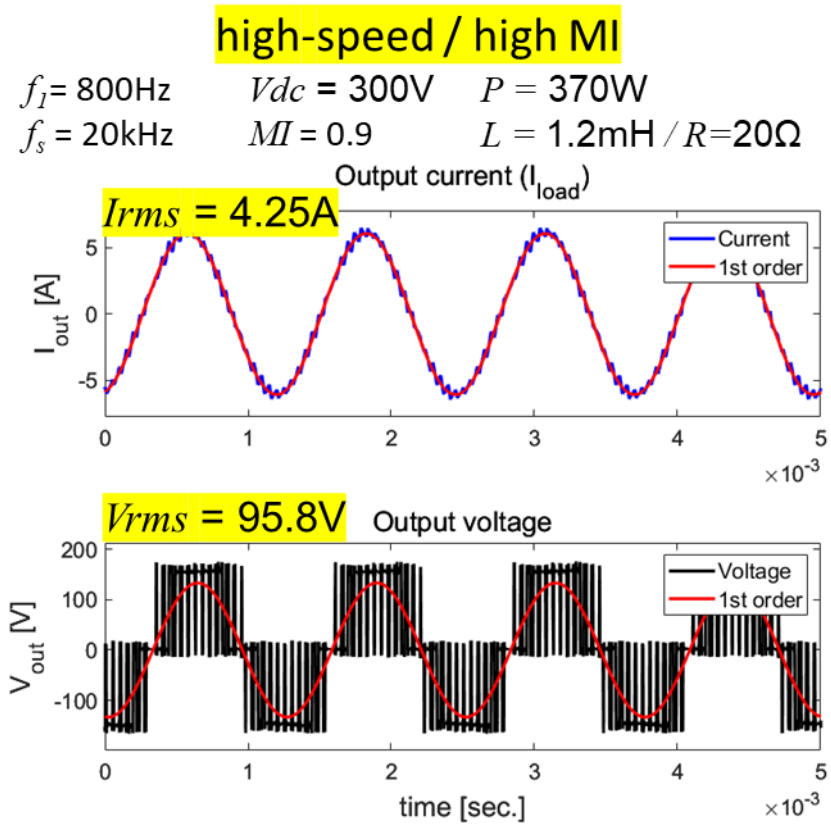
Table 6.27. Load conditions

No.	V_{DC}	R-L load	f_1	MI
1	300V	20Ω – 1.2mH	150Hz	0.5
2		4Ω – 1.2mH	800Hz	0.9

6.2.1 Efficiency vs PWM Strategies and Switching Frequency



(a)



(b)

Figure 6.84 Output load current and voltage waveform by LC-PWM at (a) load condition 1 (b) load condition 2.

Figure 6.6 presents the measured output current and voltage waveforms under the corresponding load conditions, using LC-PWM. By analyzing these output waveforms, the fundamental wave voltage and current are obtained through FFT (Fast Fourier Transform), and depicted in the graph. Under a 20kHz frequency condition, a current closely resembling a sine wave is observed at low speed, while at high speed, some harmonics are included. Figure 6.7 shows the measured efficiency at 20kHz and 40kHz under the two conditions for each PWM strategy.

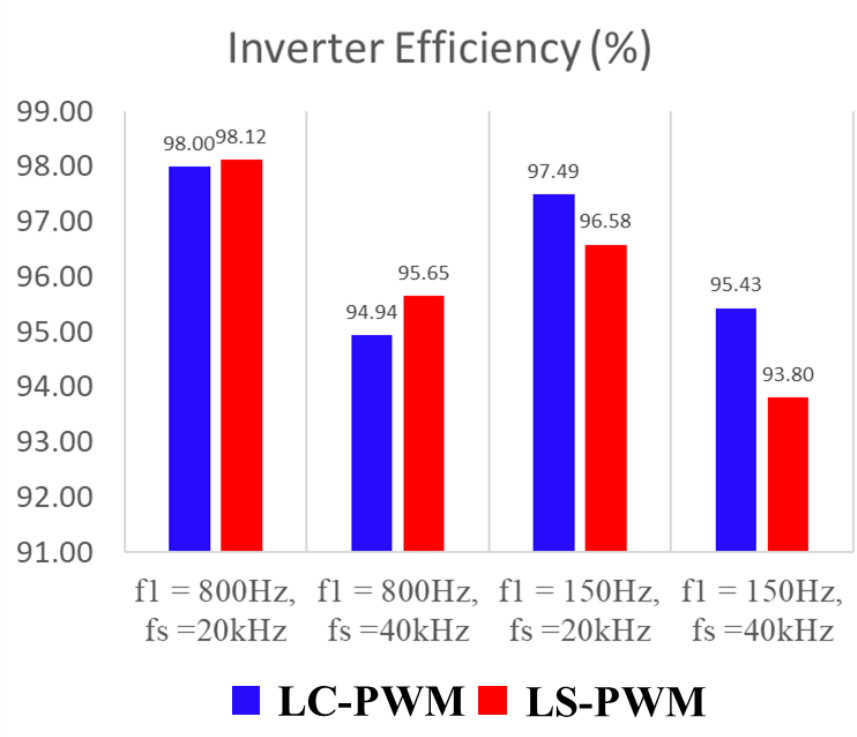


Figure 6.85 Efficiency depending on the PWM strategy and switching frequency at two load conditions.

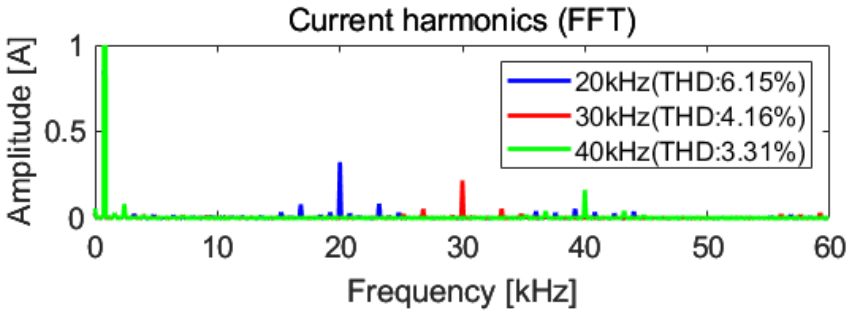


Figure 6.86 Current harmonics and THD depending on the switching frequency at 800Hz using LS-PWM

Under conditions of high operational speed at 800Hz and a MI of 0.9, the LS-PWM demonstrates a superior level of efficiency. The beneficial impact of LS-PWM on efficiency becomes even more pronounced as the switching frequency escalates. This clearly shows that the choice of PWM strategy significantly affects the performance of the system under specific load conditions. Furthermore, when testing the 150Hz load condition, a scenario that involves a relatively large current flow, the LC-PWM or Level-Clamped

Pulse Width Modulation, exhibits beneficial results under both switching frequency conditions. This clearly aligns with the results and insights that were drawn from the earlier reviewed simulation studies.

Additionally, the alteration in THD of the current waveform as a function of the rising switching frequency is represented in Figure 6.8. This depiction underscores the intrinsic relationship between these two variables and their joint impact on the overall system performance.

These observations underscore the importance of a careful and context-specific selection of PWM strategies and switching frequency in optimizing the energy efficiency of power electronics systems. They also demonstrate the potential of detailed simulation analyses in informing these decisions, ultimately contributing to the design of more energy-efficient power systems.

6.3 Summary

This chapter delves into the experimental work carried out to practically validate the ideas proposed in this thesis. A single-phase 3L-ANPC topology was constructed, and experiments were conducted under various motor load conditions, from R-L loads. The T-L load, inverter topology, and set-up conditions for each test equipment are elucidated and presented. The utilization of a RCP controller enables real-time implementation of PWM strategies and generation of a gate signal to conduct an experiment.

The findings reveal a comparison of efficiency according to the PWM strategy at two points that represent high-speed and low-speed regions; specifically, high-speed low-torque and low-speed high-torque regions. The efficiency and THD based on the switching frequency have been also compared.

As suggested in this thesis, it was affirmed that LC-PWM offers advantages in relatively low speed and high current conditions, while LS-PWM proves beneficial in relatively high frequency and low current conditions.

7 Conclusions

7.1.1 Summary of Thesis

This thesis has thoroughly examined the co-design and performance of an integrated inverter-motor system, with a particular emphasis on improving energy efficiency. The exploration began with the evaluation of drive cycles, such as the WLTP and EPA FTP-75, and delved into the energy gravity center method, which calculates representative points in the operational load spectrum to optimize the design process.

In response to the trend towards high-efficiency and high-speed operations, this thesis explored the application of WBG materials such as SiC-MOSFETs in inverters. This aligned with cutting-edge technological trends and provided a thorough review of 3L-ANPC, an advantageous multi-level topology for high voltage scenarios. The comparative benefits against 2L topologies were also scrutinized. A hybrid topology allowing for a mix of SiC or Si-IGBT in each device has been examined, along with a review of a PWM strategy suitable for this topology. Specifically, All-SiC, 2SiC-4Si hybrid topologies, and the corresponding LC-PWM and LS-PWM have been proposed and evaluated to ascertain which conditions they are advantageous in, under various drive load conditions.

This research also considered advanced designing method for IPMSM, a commonly utilized motor in electric drive systems. It scrutinized how the parameters of the inverter and the motor design could mutually influence improvement. A significant concept proposed is that increasing the switching frequency, like the application of WBG, enhances the design flexibility in terms of the number of poles and turns of the motor. This could, in turn, reduce system energy loss through a more energy-efficient motor design.

The development of an inverter co-simulation model linked to FEA based motor analysis enabled the prediction of the entire system's loss. This model served as an active tool for optimizing energy efficiency.

The inverter design study has revealed that different results could be obtained depending on the devices used within the same 3L-ANPC topology. Also, the effectiveness of PWM strategies varied with the load conditions. LC-PWM, for instance, reduced conduction loss and proved advantageous in regions where conduction loss is dominant

over switching loss, particularly in mid- and high-torque mid-low-speed regions. Conversely, LS-PWM is beneficial at high-speed and low-torque regions, which is mainly influenced by switching loss.

Furthermore, a comprehensive methodology for reducing energy loss has demonstrated through case studies in 400V PHEV systems and 800V BEV systems. The approach considers various design parameters such as different PWM strategies, inverter topology, switching frequency, and the number of poles and turns in motors and other geometry of the motor. An innovative idea of hybrid modulation, incorporating a mix of the two PWM strategies throughout the entire range, has been presented.

Finally, the central concept of this research has been validated through the actual prototype of a single phase 3L-ANPC. This thesis presents a significant contribution to the ongoing efforts to improve the efficiency and performance of electric vehicle technology, and offers a path forward for further innovations in this field.

7.1.2 Further Potential Studies

The research conducted in this study has laid the foundation for several interesting paths that could be explored further. Here are some possible directions for future research:

- Thermal Estimation Model Development: A significant area where loss prediction can be improved is in the development of a thermal prediction model. Numerous thermal prediction models are currently under investigation, and a comprehensive model that combines them could enhance loss prediction accuracy. Not just the WBG elements, but also various motor parts may degrade due to heat, and the various losses discussed in this study may be impacted by temperature fluctuations. While this research has performed loss predictions under high temperature conditions, accurate temperature forecasting could greatly facilitate the development of more efficient systems. In addition, more precise thermal predictions can also assist in making informed projections about the reliability of the device and, by extension, the entire system. Understanding how components and the system as a whole will respond to different thermal conditions can help in designing systems that are not only efficient but also

reliable under a wide range of operating conditions. This could help engineers design systems that continue to perform optimally even under extreme conditions, thereby extending the life of the devices and reducing maintenance and replacement costs.

- Effect Study on Parasitic Component: Another area for potential further research is the impact of parasitic components on system performance. Parasitic components, such as parasitic capacitances and inductances, are intrinsic properties in electrical systems and can affect the operation of the system in significant ways. For instance, they can cause unwanted oscillations, degrade system efficiency, or even lead to system instability in some cases. A detailed study on the effect of parasitic components in inverters and motors could provide valuable insights. Understanding their impact on the electrical performance, efficiency, and reliability of systems can lead to better design strategies that mitigate the adverse effects of these parasitic components. This can include optimizing component layout, improving circuit design, or developing advanced control strategies. In particular, for high-frequency operations as in the case of WBG devices, the effects of parasitic components become increasingly prominent. Therefore, the study of parasitic components in such scenarios could provide critical knowledge for the design of more efficient and reliable high-frequency systems. This research could also lead to the development of models that accurately account for the effects of parasitic components, leading to better system simulation and design tools.
- Optimization using AI and Deep Learning: Artificial Intelligence (AI) could significantly contribute to the advancement of parameter optimization in the context of inverter and motor design. Advanced machine learning techniques, such as genetic algorithms, neural networks, or reinforcement learning, could be applied to optimize various parameters to enhance system performance and efficiency. This optimization process could involve tuning various design parameters, such as switching frequency, number of poles and turns in motors,

topology configuration, and PWM strategy. This could also include optimizing system configurations under various load conditions.

By exploring these and other research avenues, we can continue to push the boundaries of what's possible in energy efficiency, driving improvements in electric vehicles, renewable energy systems, and beyond.

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